1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,J45

DVT 8/6/2013

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0456	1	SCHEM,MLB,J45	SCH	CRITICAL	
820-3662	1	PCBF,MLB,J45	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Tue Aug 6 17:09:28 2013

DRAWING TITLE
<PART_DESCRIPTION>

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DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0067	COMMON PARTS,MLB,J45	J45_COMMON
985-0045	DEV BOM,MLB,J45	J45_DEVEL:ENG
639-4822	PCBA,MLB,BETTER,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600_S
639-4823	PCBA,MLB,BETTER,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600
639-4828	PCBA,MLB,BETTER,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600_S
639-4829	PCBA,MLB,BETTER,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600
639-4834	PCBA,MLB,BETTER,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600_S
639-4835	PCBA,MLB,BETTER,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600
639-4840	PCBA,MLB,BEST,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600_S
639-4841	PCBA,MLB,BEST,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600
639-4846	PCBA,MLB,BEST,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600_S
639-4847	PCBA,MLB,BEST,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600
639-4852	PCBA,MLB,BEST,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600_S
639-4853	PCBA,MLB,BEST,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600
639-4858	PCBA,MLB,CTO,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600_S
639-4859	PCBA,MLB,CTO,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600
639-4864	PCBA,MLB,CTO,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600_S
639-4865	PCBA,MLB,CTO,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600
639-4870	PCBA,MLB,CTO,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600_S
639-4871	PCBA,MLB,CTO,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600

J45 BOM Groups

BOM GROUP	BOM OPTIONS
J45_COMMON	ALTERNATE,COMMON,J45_COMMON1,J45_COMMON2,J45_PROGPARTS
J45_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUPEG:X16,S2_PWR:S0
J45_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45_PVB	BKLT:PROD,SENSOR_NONPROD:N
J45_PROGPARTS	SMC_PROG:EVT,BOOTROM_PROG:DVT,TBTROM:PROG,TPAD_PSOC:PROG
J45_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,DDRVREF_DAC,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,CAM_XTAL:YES
J45_DEVEL:FSB	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,SENSOR_NONPROD_R
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	CRW,SR18J,,PRQ,C0,2.0,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S4600	1	CRW,SR18H,PRQ,C0,2.3,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BEST
337S4624	1	CRW,SR1BS,PRQ,C0,2.6,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,QEWV,LPT-M,HM87,C2,SR199,PRQ,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S0667	16	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	HYNIX_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	SAMSUNG_1600_S
333S0703	16	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	ELPIDA_1600_S
333S0660	16	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600_S
333S0667	32	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	SAMSUNG_1600
333S0703	32	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	ELPIDA_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600_S	HYNIX_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600_S	SAMSUNG_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600_S	ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600_S	MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM:HYNIX_1600	HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600	SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600	ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600	MICRON_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0067	1	J45 MLB BASE BOM	BASE	CRITICAL	BASE_BOM
985-0045	1	J45 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S3919	1	IC,EPROM,Falcon RIDGE(V13.9)J44/45	U2890	CRITICAL	TBTROM:PROG
337S4587	1	IC,TP PSOC, QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK
341S3856	1	IC,TRKPD/KYBD,PSOC(V225)	U4801	CRITICAL	TPAD_PSOC:PROG

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3902	1	IC,SMC-B1,EXT,V2.12A54,EVT,J45	U5000	CRITICAL	SMC_PROG:EVT
341S3741	1	IC,SMC-A3,SCPL,EXT,VXXXX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBIT,8SOP,FUSE=1	U6100	CRITICAL	BOOTROM_BLANK:MACRONIX
335S0812	1	IC,SPI SRL 50MHZ,FLASH,64MBIT,SOIC8	U6100	CRITICAL	BOOTROM_BLANK:NUMONYX
341S3763	1	IC,EFI ROM(VXXXX)PROTO 0,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S3780	1	IC,EFI ROM(V0035)PRE-PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PRE-PROTO1
341S3793	1	IC,EFI ROM(V0041)PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3811	1	IC,EFI ROM(V00xx)PROTO 2,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S3890	1	IC,EFI ROM(V0100)PROTO3-J45 &EVT-J45	U6100	CRITICAL	BOOTROM_PROG:EVT
341S3929	1	IC,EFI ROM(Vxxxx)DVT-J45	U6100	CRITICAL	BOOTROM_PROG:DVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7845	1	MBP BARCODE LABEL	LABEL	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0241		ALL	Cyntec alt to TFT
376S1032	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
128S0371	128S0376		ALL	Kemet alt to Sanyo
333S0629	333S0703		ALL	Elpida F die alt
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000
311S0649	311S0541		ALL	ON alt to Toshiba (U2030, U7001)

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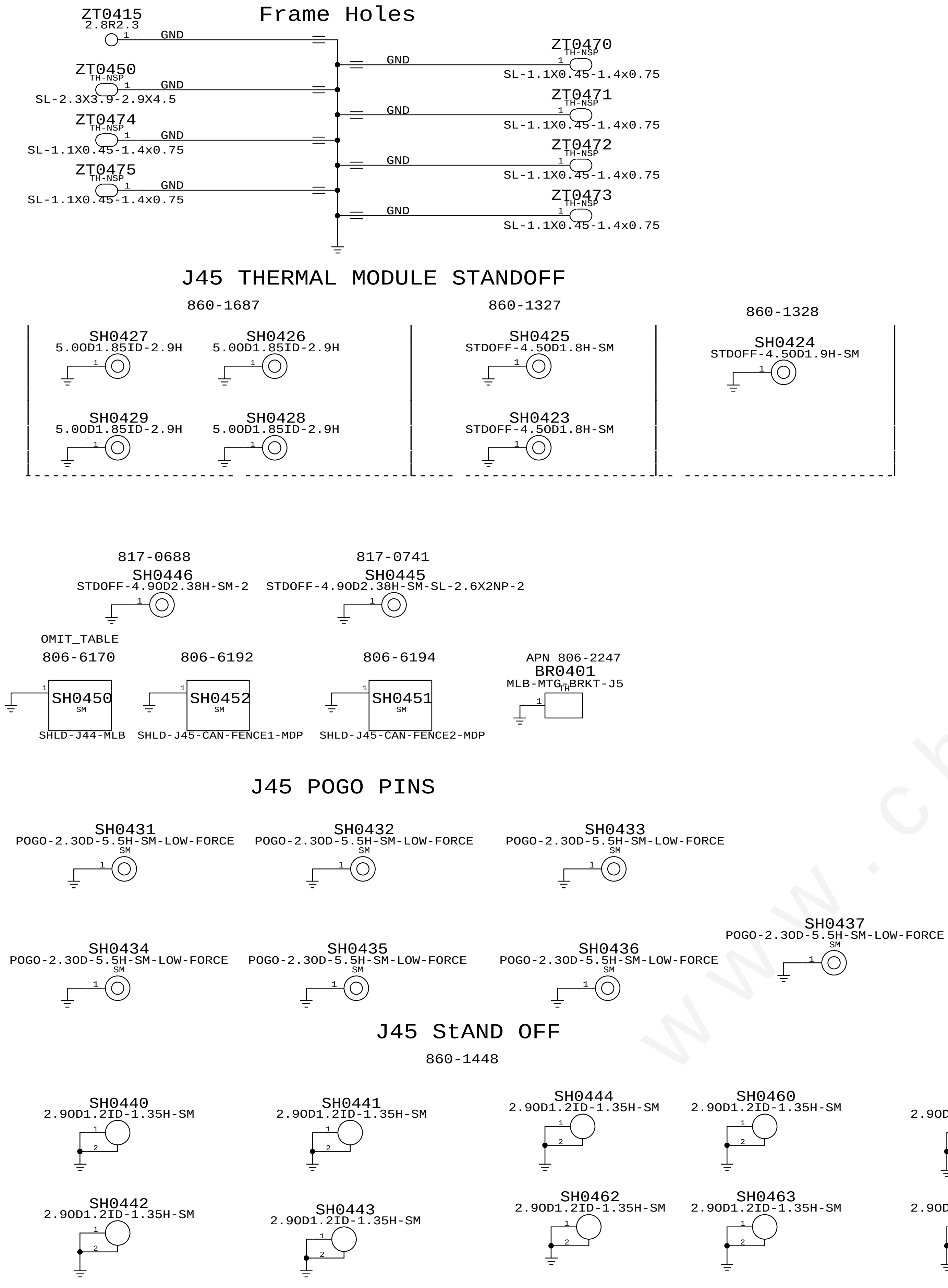
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BOM Configuration

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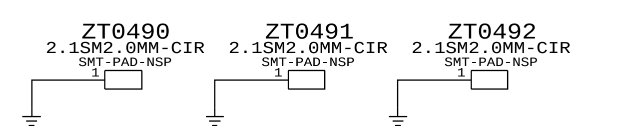
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SMT GND TEST PONTS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
725-1807	1	INSULATOR,REAR,MLB,J45	REAR_INSULATOR	CRITICAL	
725-1877	1	INSULATOR,CPU,J45	CPU_INSULATOR	CRITICAL	
725-1787	1	INSULATOR,PCH,J15	PCH_INSULATOR	CRITICAL	
806-6193	2	CAN COVER,mDP	CAN_COVER1, CAN_COVER2	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	
806-9391	1	SHIELD CAN, USB,J45	SH0450	CRITICAL	

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PD Parts

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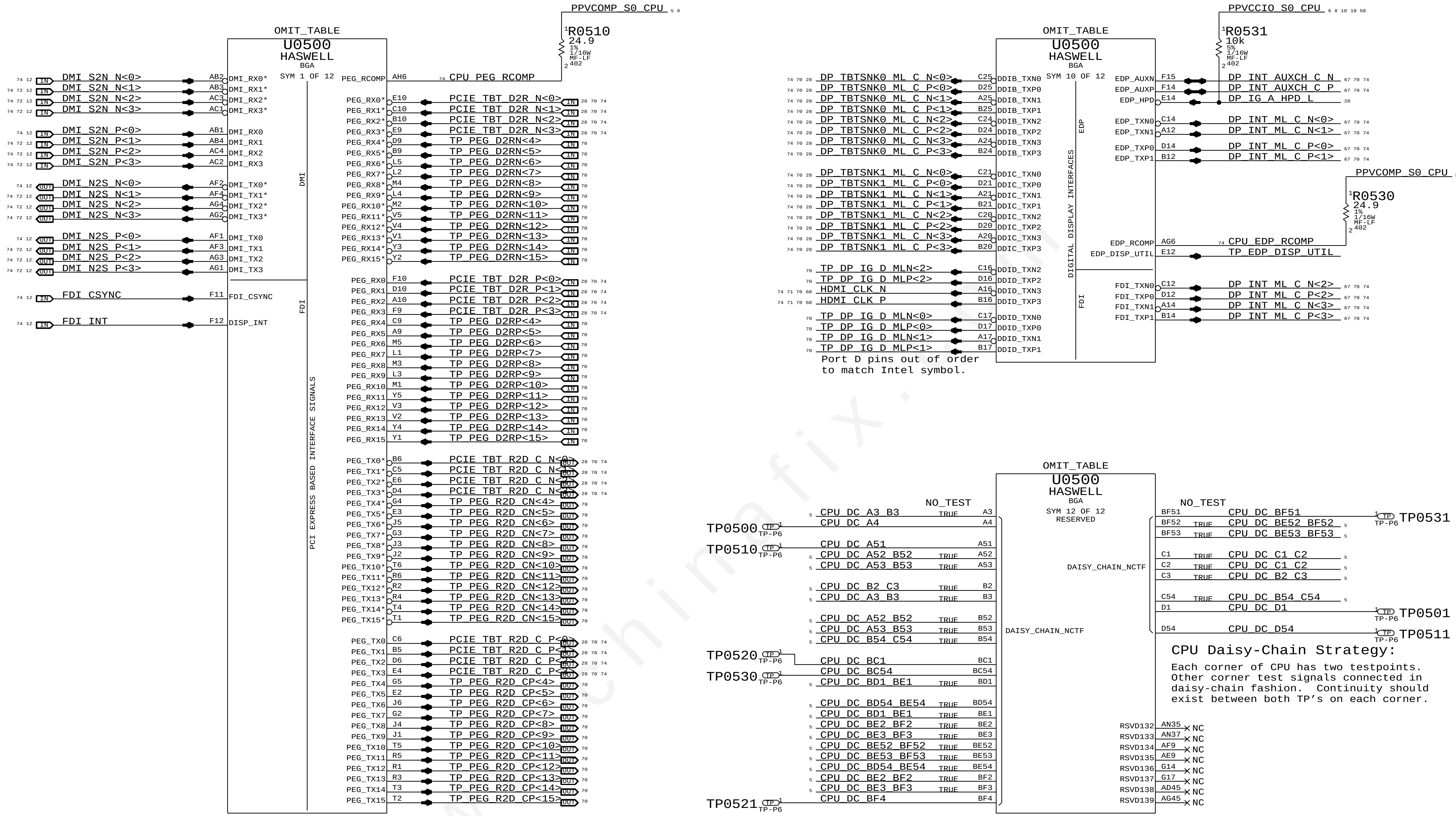
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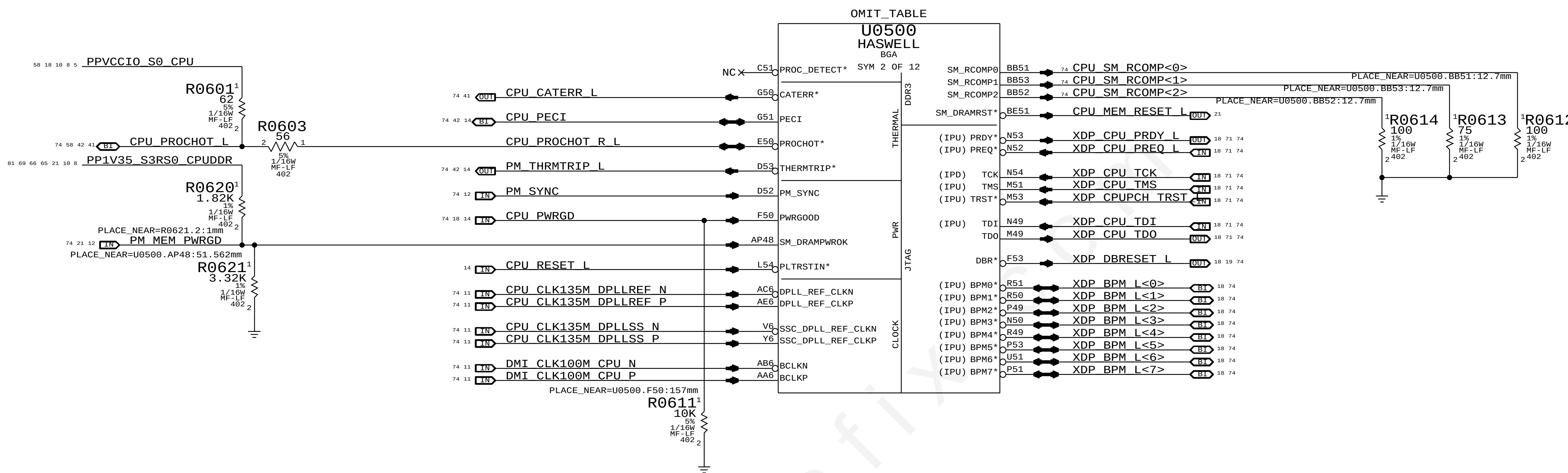
CPU DMI/PEG/FDI/RSVD

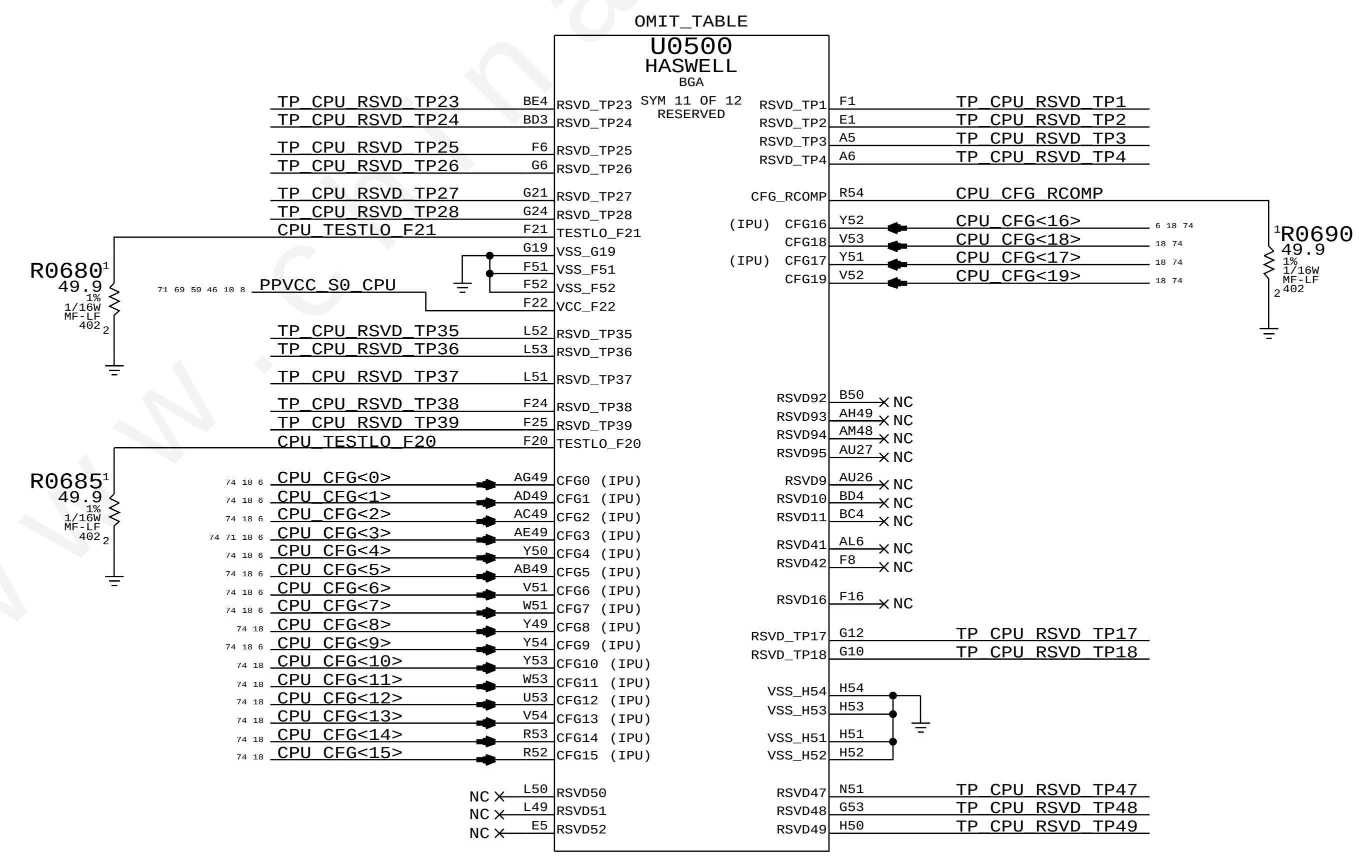
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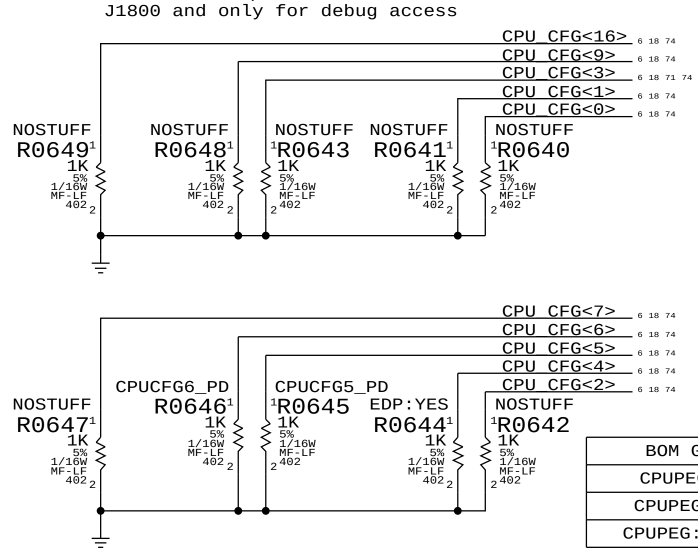
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CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

These can be placed close to
J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CPUPEG:X16	
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

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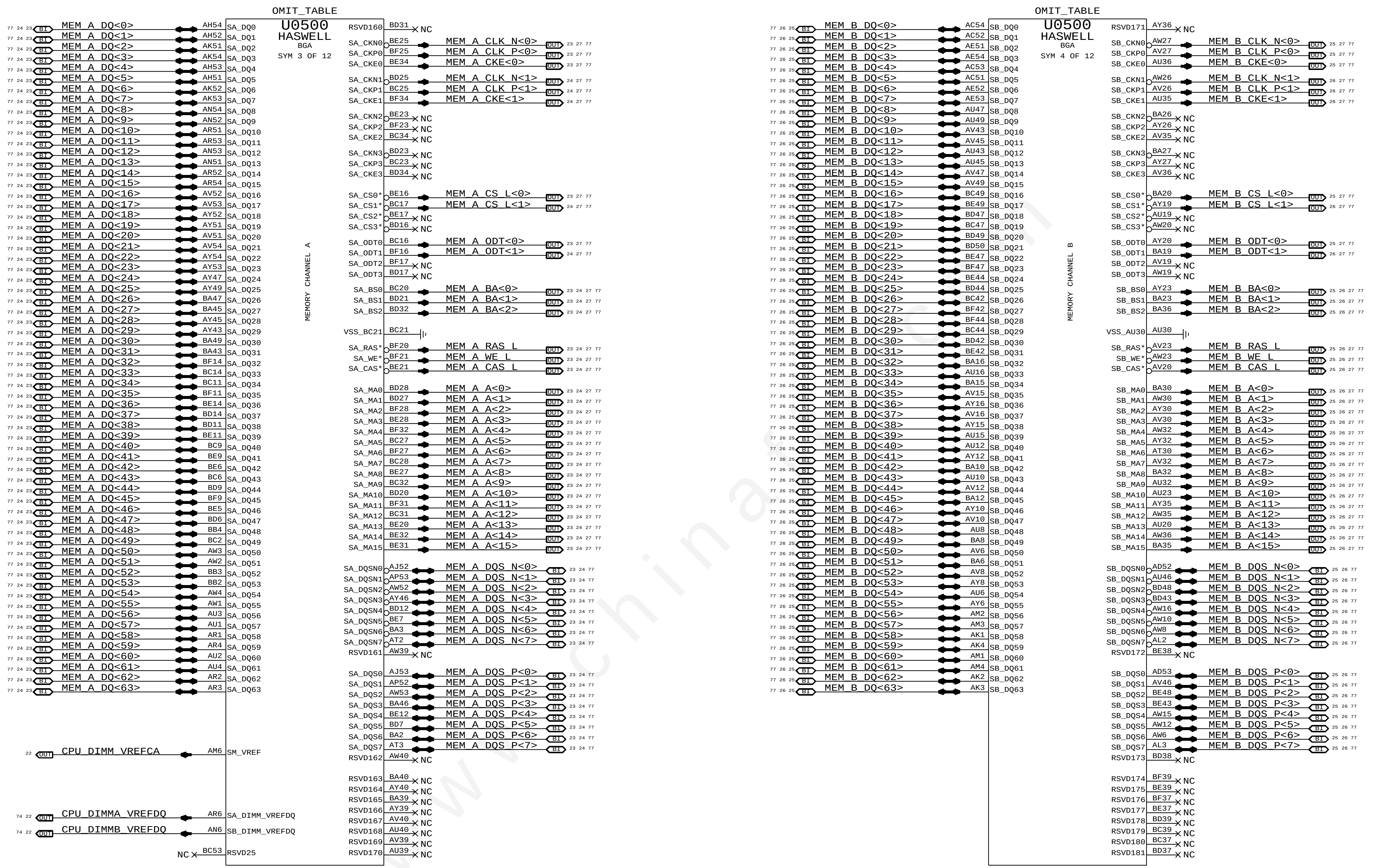
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CPU Clock/Misc/JTAG/CFG

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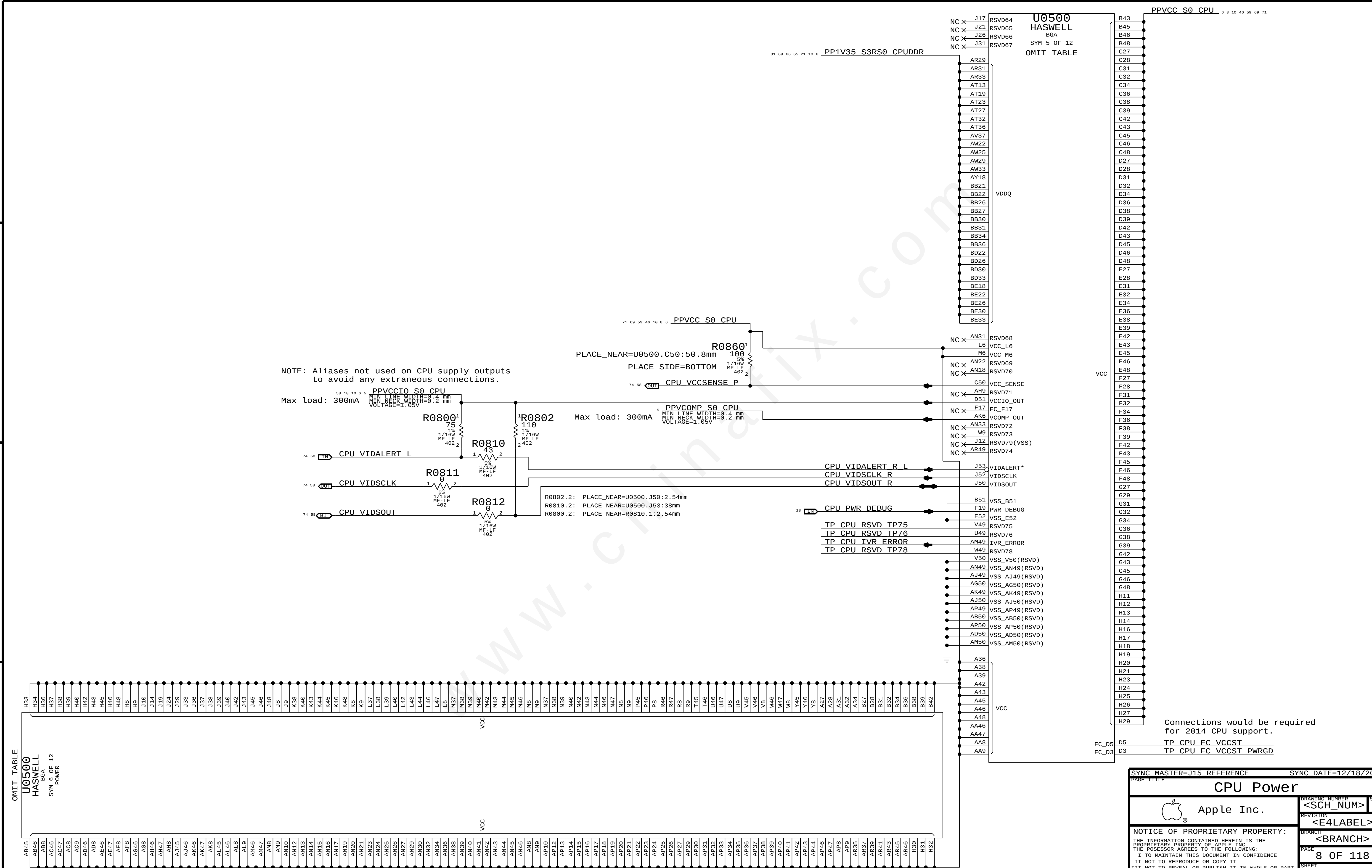
CPU DDR3 Interfaces

Apple Inc.

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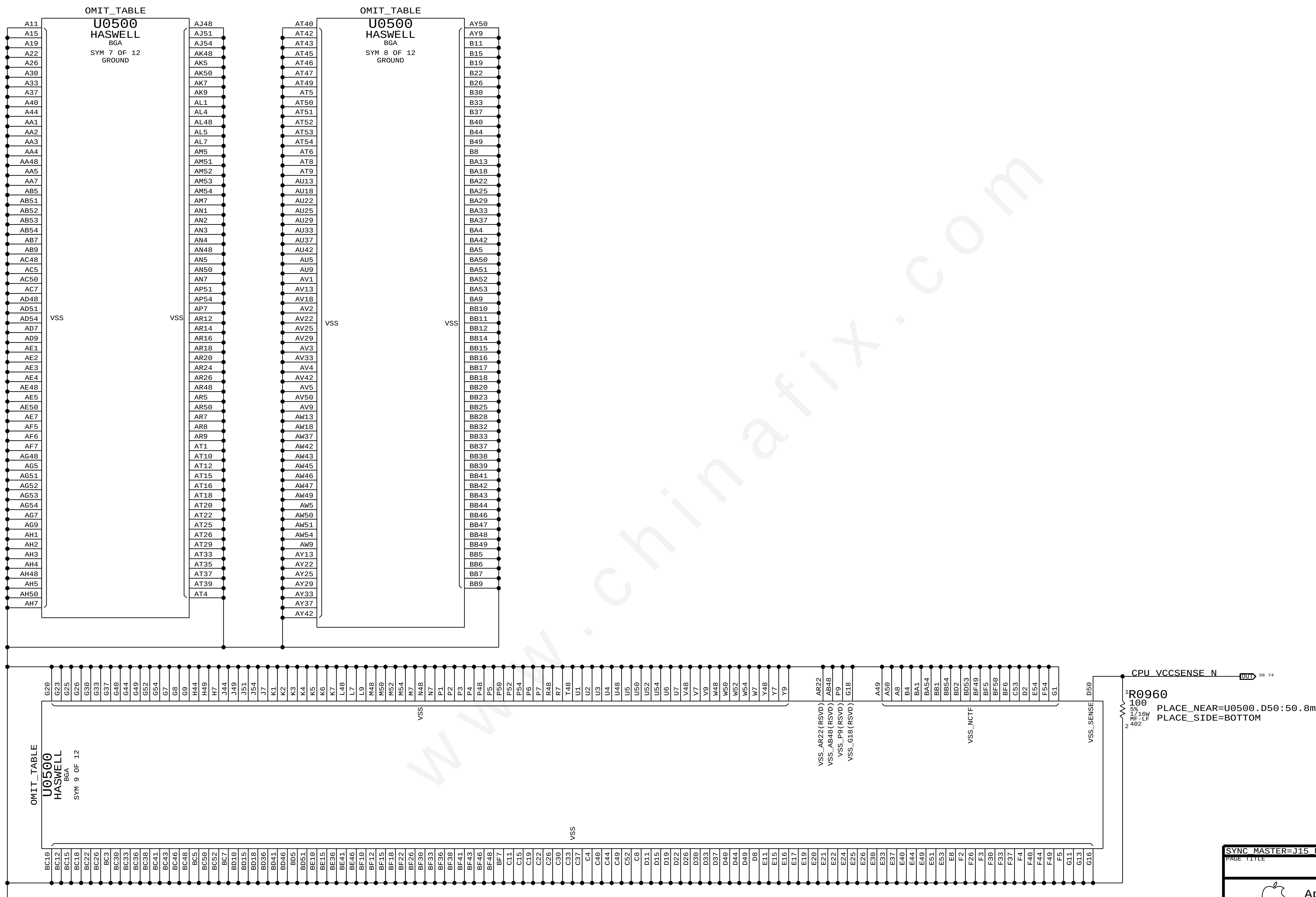
CPU Power

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CPU Ground

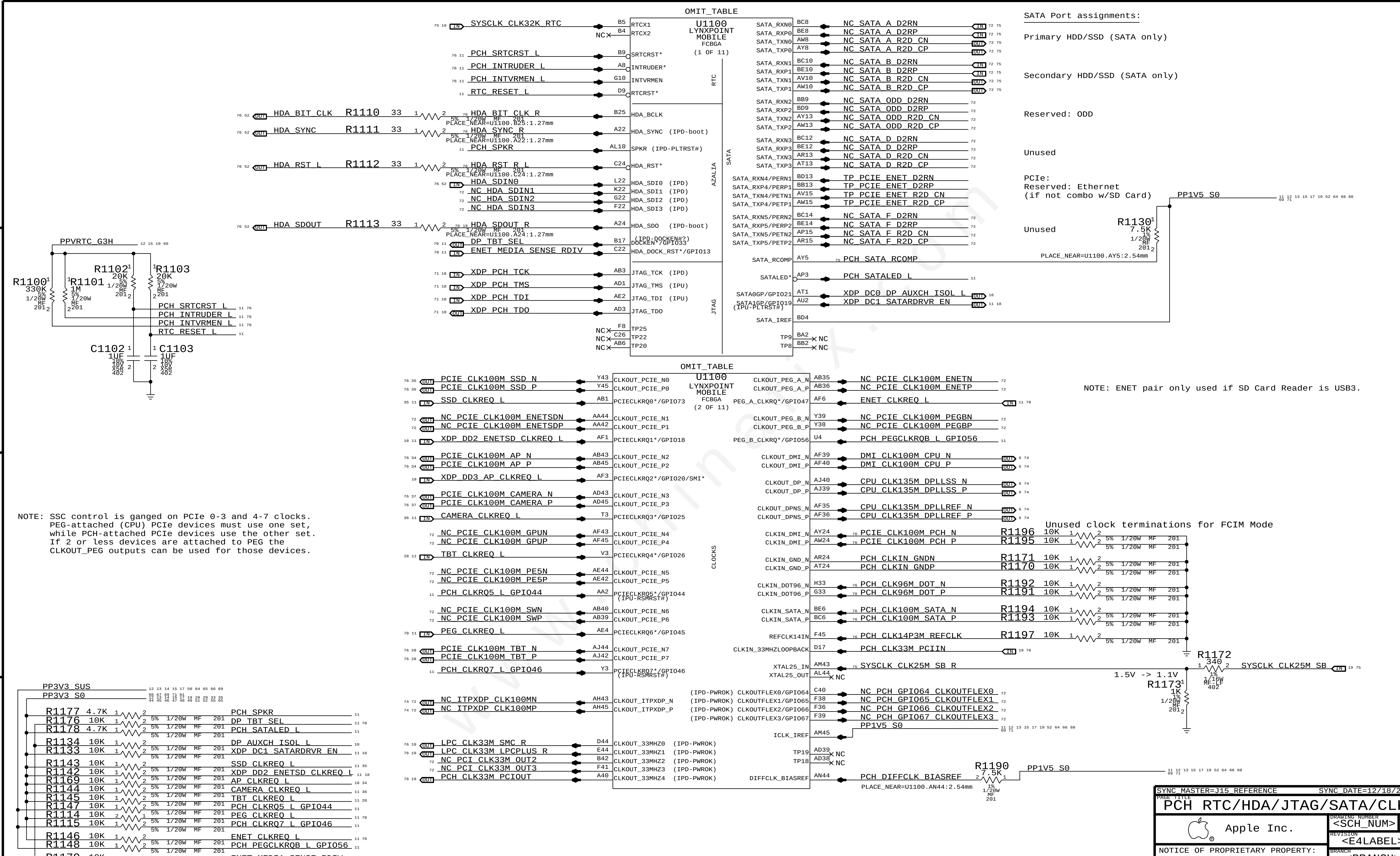
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CPU VCORE Decoupling
Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 8x 210uF(2x nostuff) 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402
PPVCC_S0_CPU
PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500
C1000 C1001 C1002 C1003 C1004 C1005 C1006 C1007 C1008 C1009 C1010 C1011 C1012 C1013 C1014 C1015 C1016 C1017 C1018 C1019
1UF 10% 10V X6S-CERM 0402
PLACEMENT_NOTE (C1020-C1023):
Place near U0500 on bottom side
CAPs for Acoustic control (C109A-C102D)
NO STUFF
C1020 C1021 C1022 C1023 C109A C109B C109C C109D C109E C109F C101A C101B C101C C101D C101E C101F C102A C102B C102C C102D
20UF 20% 4V X5R-CERM 0402-2
PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.
CRITICAL
C1024 C1025 C1026 C1027 C1028 C1029 C1030 C1031 C1032 C1033 C1034 C1035 C1036 C1037 C1038 C1039 C1040 C1041 C1042 C1043 C1044 C1045
20UF 20% 4V X5R-CERM 0402-2
PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.
C1046 C1047 C1048 C1049 C1050 C1051 C1052 C1053 C1054 C1055 C1056 C1057 C1058 C1059 C1060 C1061 C1062 C1063 C1064 C1065 C1066 C1067
20UF 20% 4V X5R-CERM 0402-2
PLACEMENT_NOTE (C1068-C1076:
CAPs for Acoustic control (C102E-C103F)
C1068 C1069 C1070 C1071 C1072 C1073 C1074 C1075 C1076 C1077
210UF 20% 2.5V POLY-TANT CASE-B2S
C102E C102F C103A C103B C103C C103D C103E C103F
20UF 20% 4V X5R-CERM 0402-2
CPU VDDQ Decoupling
Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
PP1V35_S3RS0_CPUDDR
PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500
C1080 C1081 C1082 C1083 C1084 C1085 C1086 C1087 C1088 C1089
1UF 10% 10V X6S-CERM 0402
PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side
C1090 C1091 C1092 C1093 C1094 C1095 C1096 C1097
10UF 20% 4V X6S-CERM 0603
PLACEMENT_NOTE (C1098-C1099):
CRITICAL
C1098 C1099
330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)
CPU VCCIO Decoupling
Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)
PPVCCIO_S0_CPU
C1079
0.01UF 10% 16V X7R-CERM 0402
NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.
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CPU Decoupling
Apple Inc.
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NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

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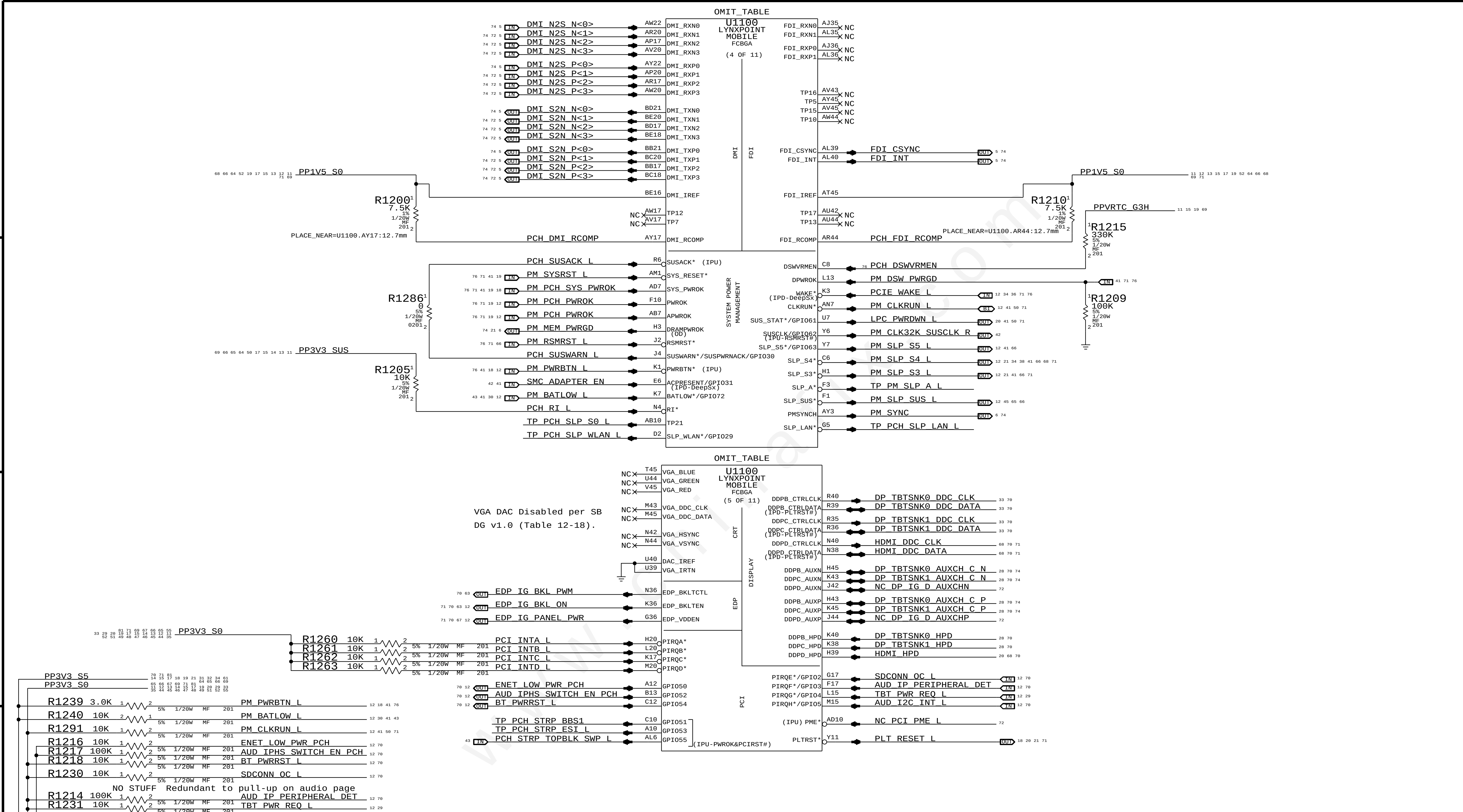
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PCH RTC/HDA/JTAG/SATA/CLK

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PCH DMI/FDI/PM/GFX/PCI

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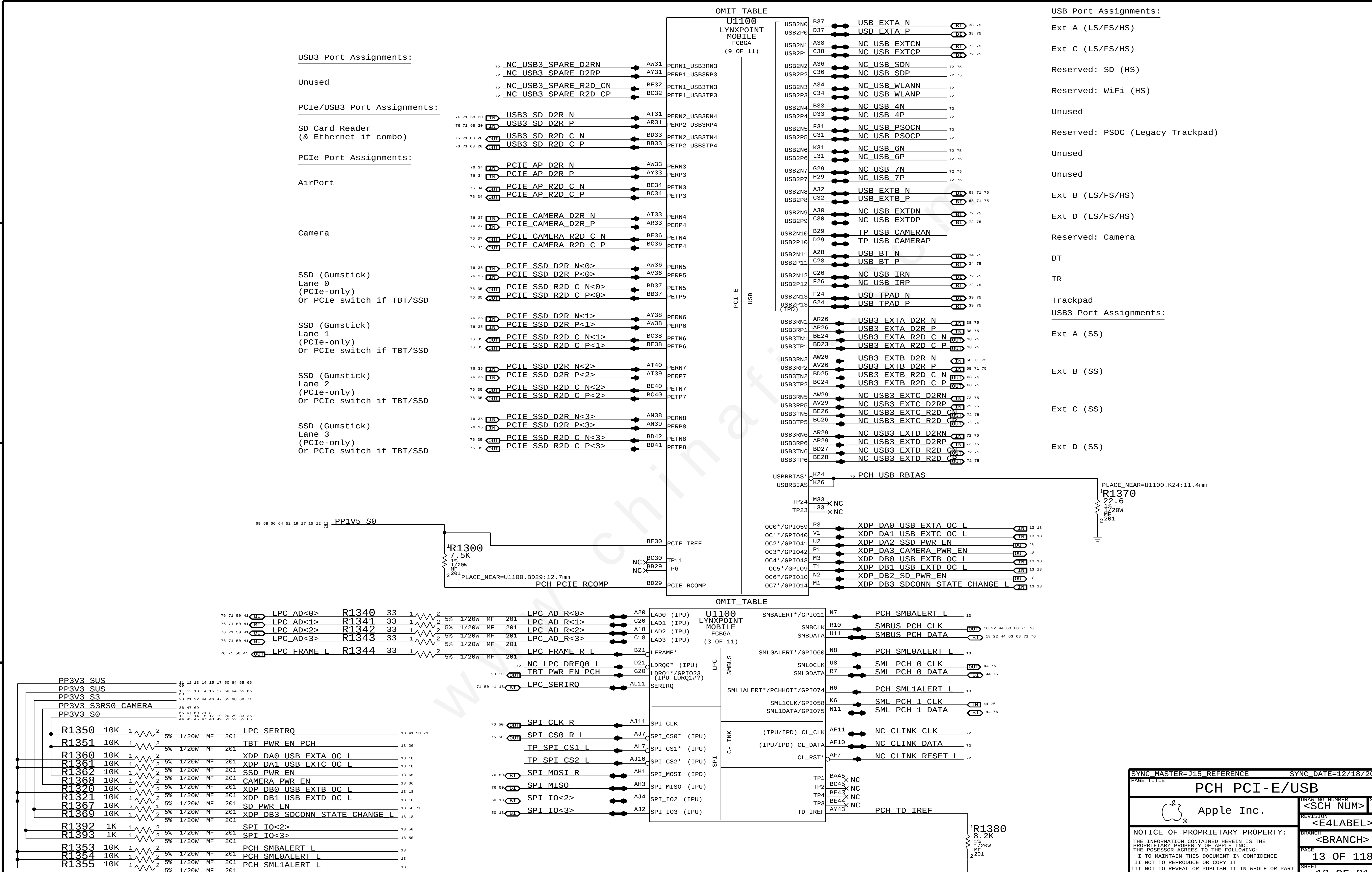
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PCH PCI-E/USB

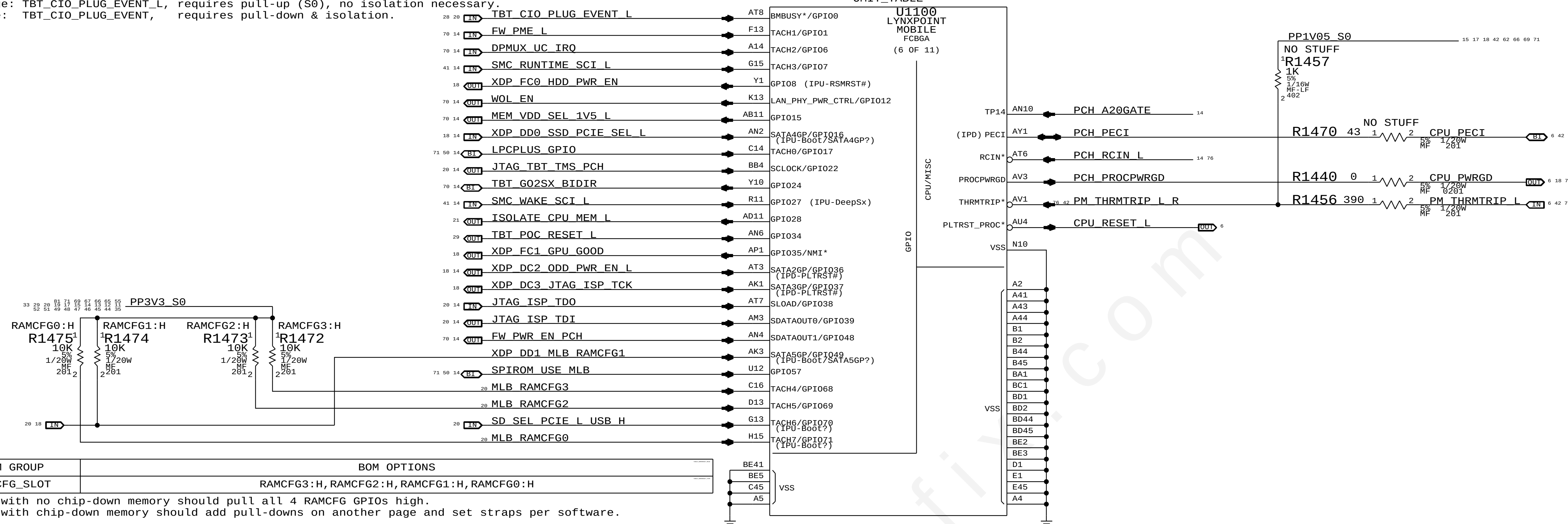
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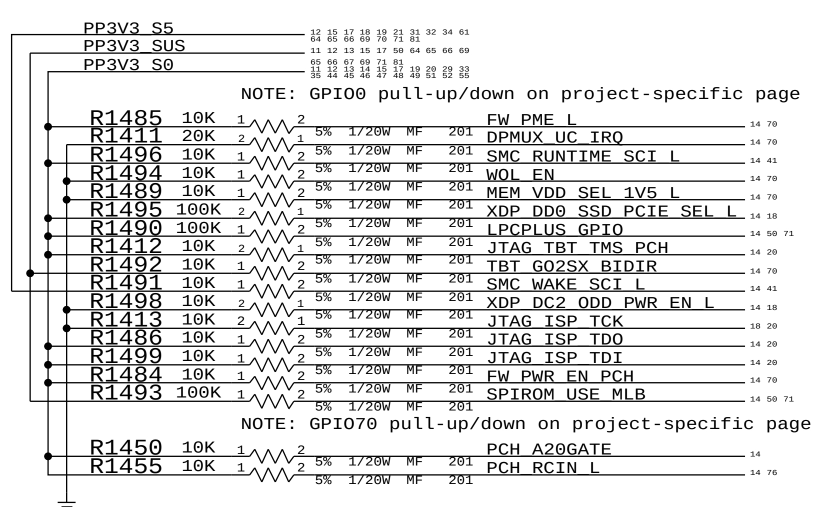
BRANCH <BRANCH>

Pull-up/down on chipset support page (depends on TBT controller)
Redwood Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

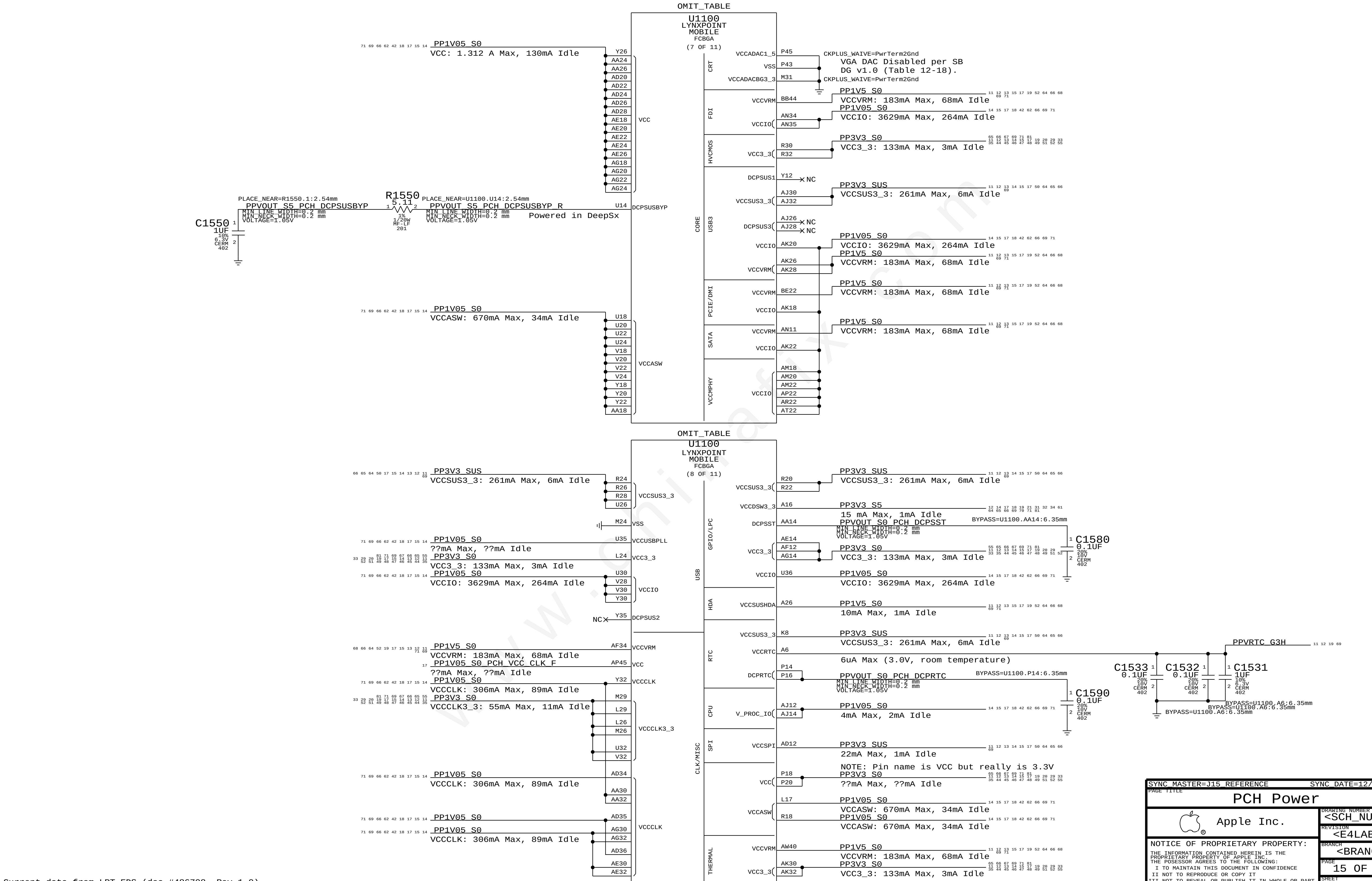


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PCH GPIO/MISC/NCTF

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Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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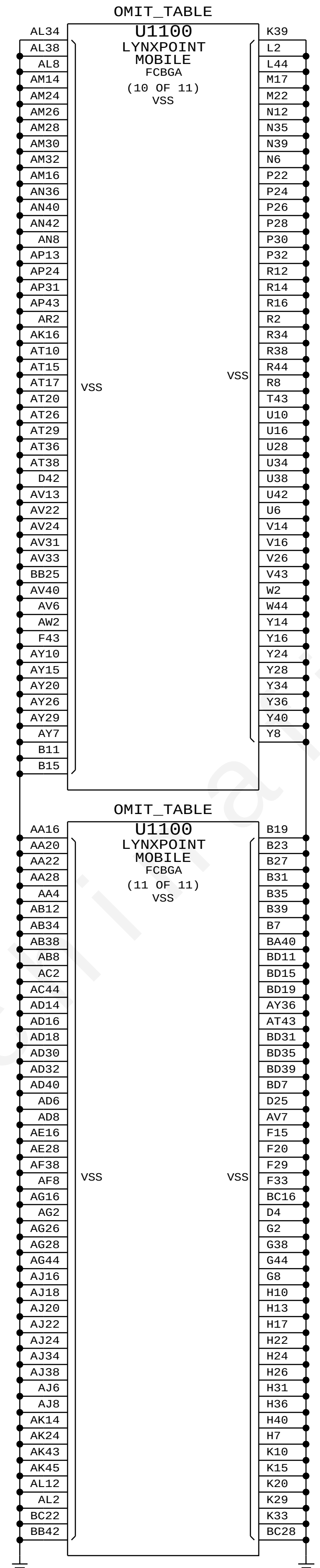
PCH Power

DRAWING NUMBER <SCH_NUM> SIZE D

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SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH Grounds

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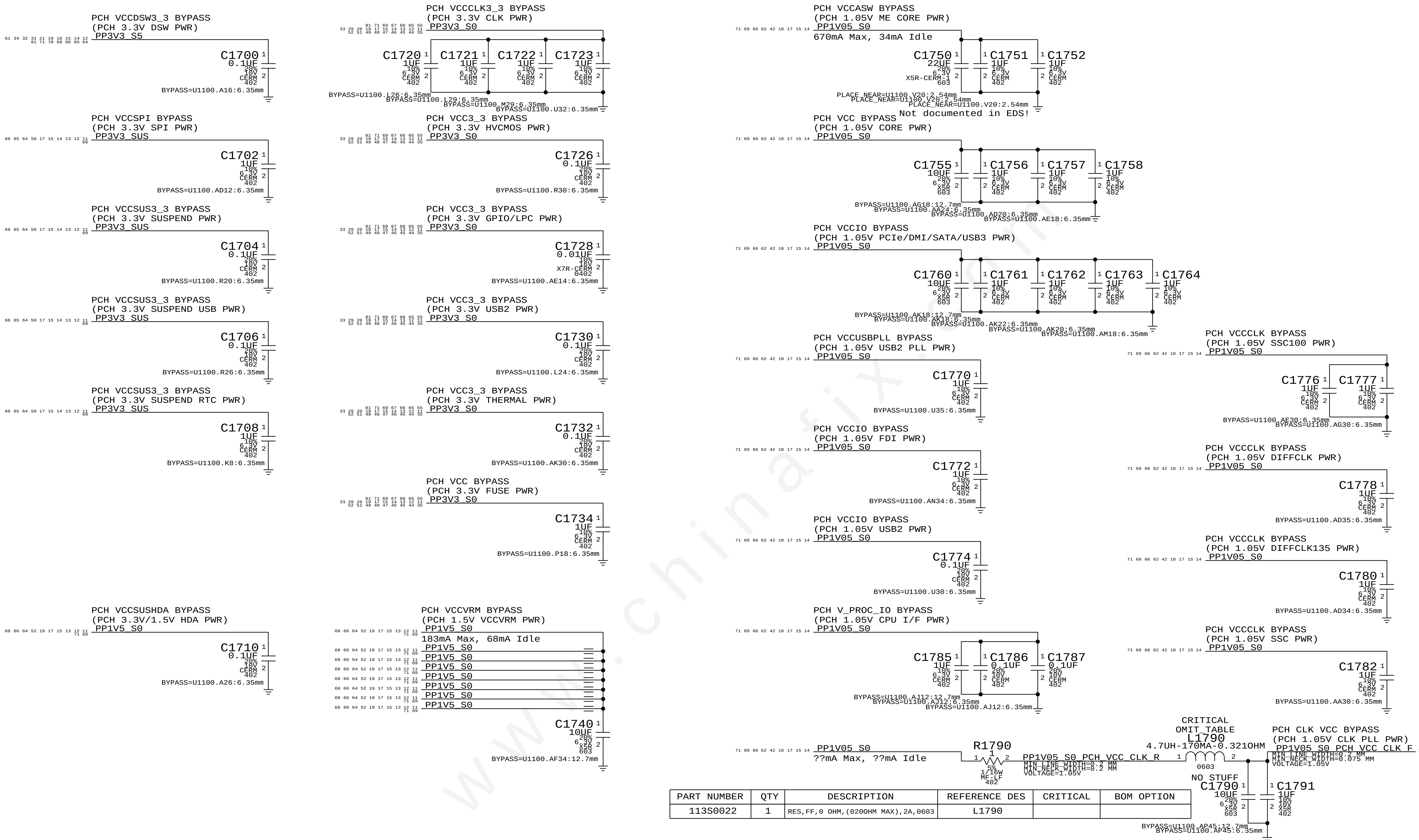
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020HM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

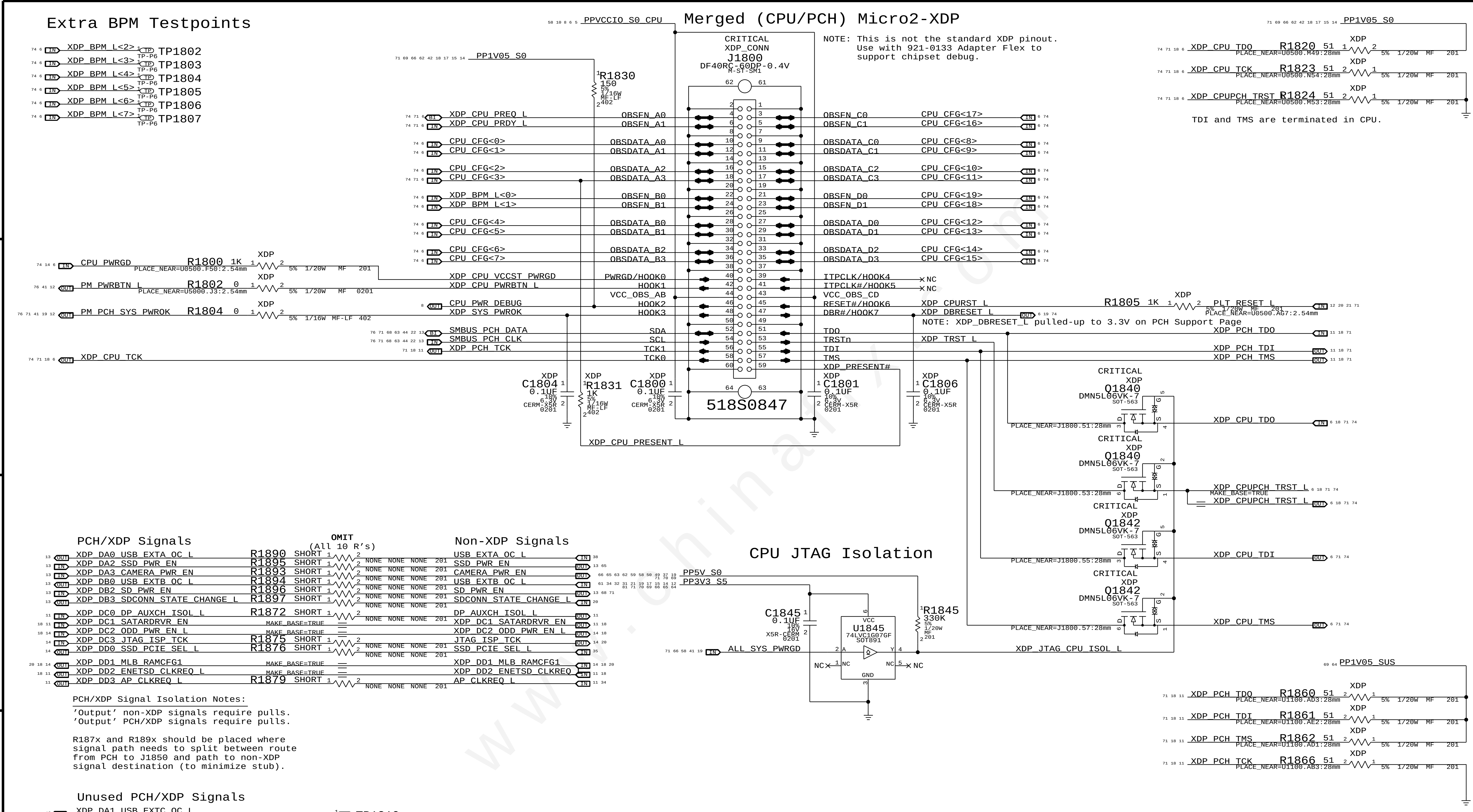
PCH DECOUPLING

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PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

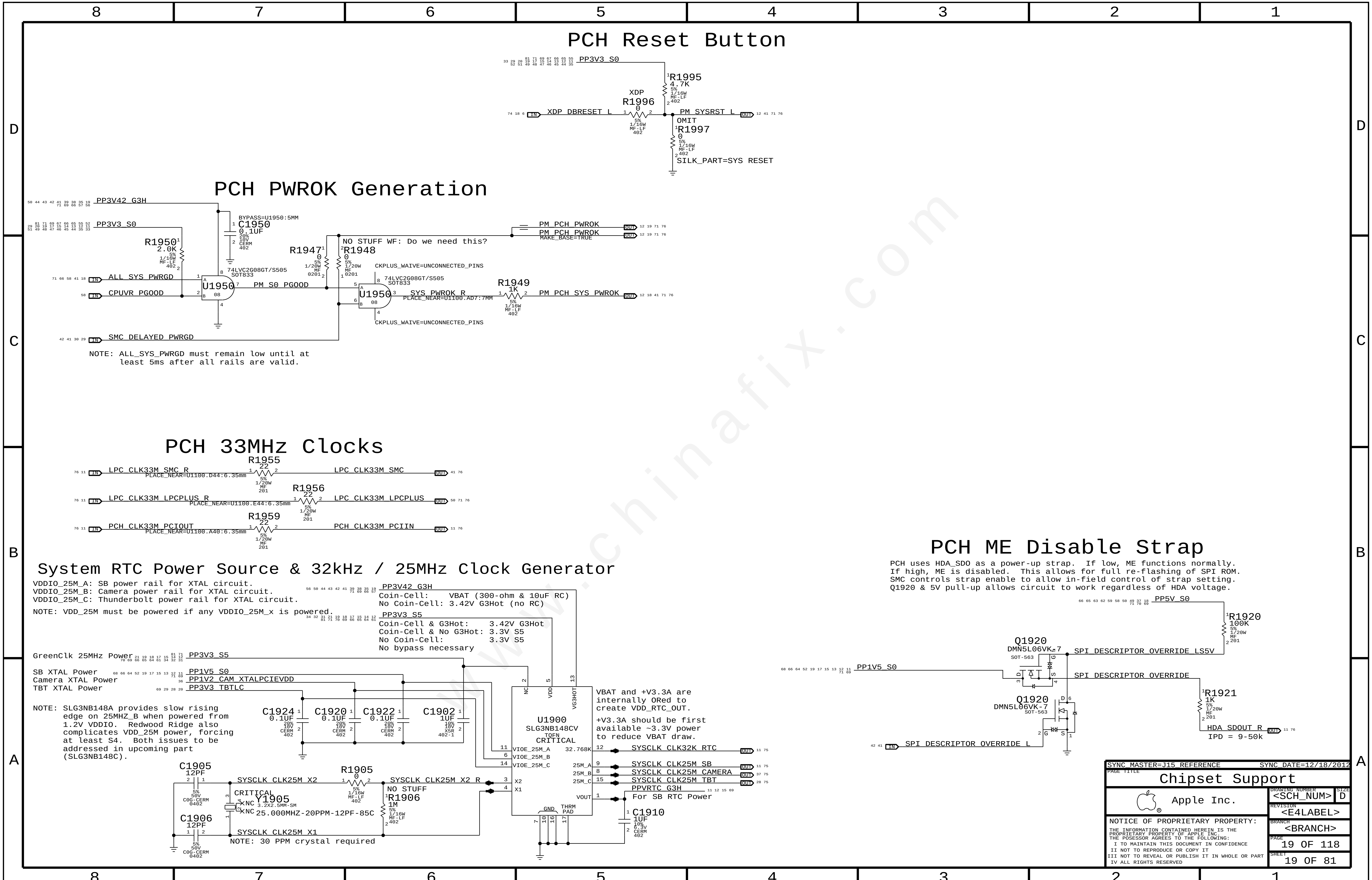
PAGE TITLE: CPU & PCH XDP

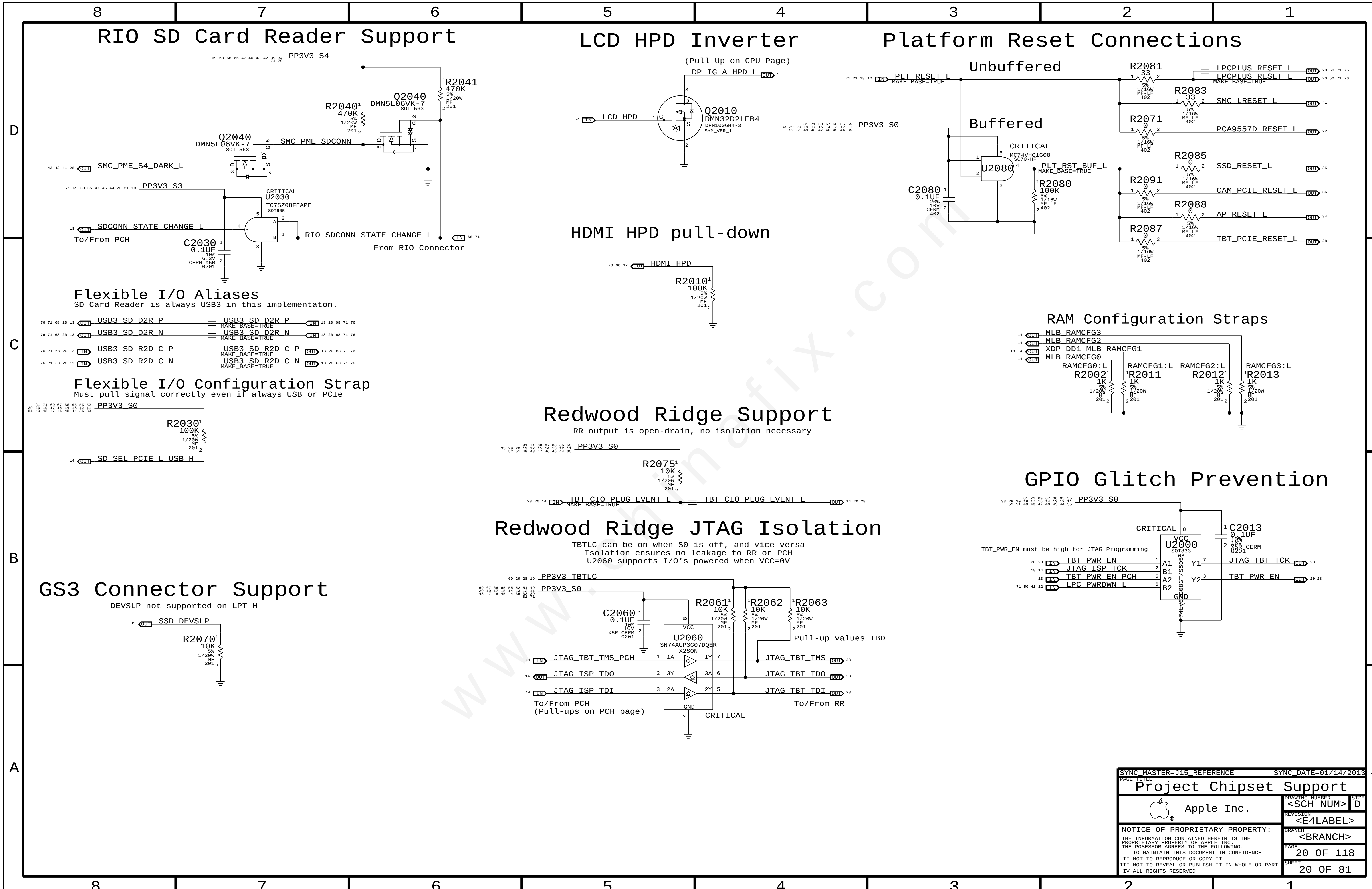
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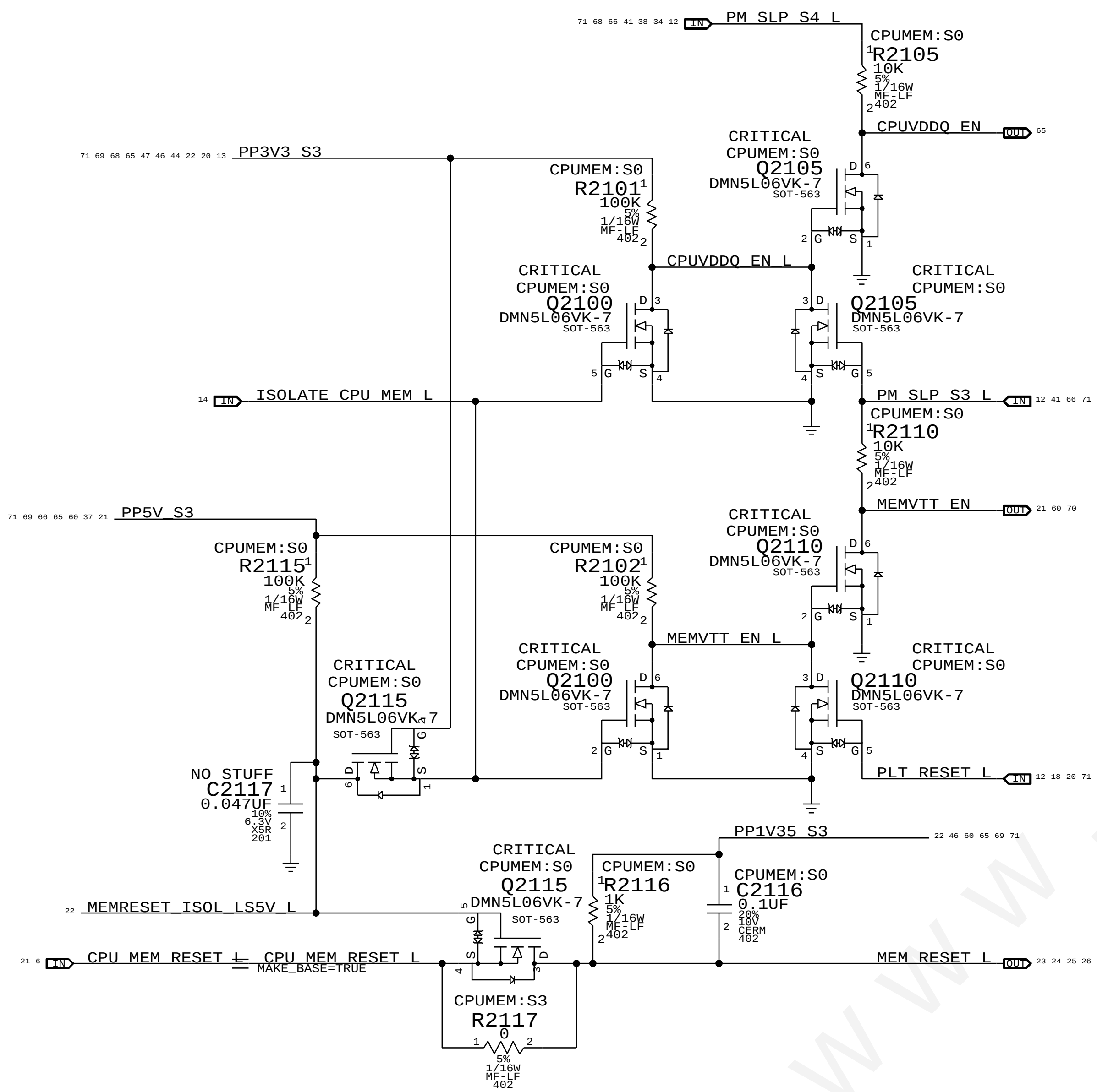

PCH Reset Button
PP3V3_S0
R1995
4.7K
5%
1/16W
MF-LF
402
XDP
R1996
0
XDP_DBRESET_L
PM_SYSRST_L
OMIT
R1997
0
SILK_PART=SYS RESET
PCH PWROK Generation
PP3V42_G3H
PP3V3_S0
BYPASS=U1950:5MM
C1950
0.1UF
20%
10V
CERM
402
R1950
2.0K
R1947
0
R1948
0
NO STUFF WF: Do we need this?
PM_PCH_PWROK
MAKE_BASE=TRUE
ALL_SYS_PWRGD
CPUVR_PGOOD
74LVC2G08GT/S505
SOT833
U1950
PM_S0_PGOOD
CKPLUS_WAIVE=UNCONNECTED_PINS
R1949
1K
SYS_PWROK_R
PLACE_NEAR=U1100.AD7:7MM
PM_PCH_SYS_PWROK
SMC_DELAYED_PWRGD
NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.
PCH 33MHz Clocks
R1955
22
LPC_CLK33M_SMC_R
PLACE_NEAR=U1100.D44:6.35mm
LPC_CLK33M_SMC
R1956
22
LPC_CLK33M_LPCPLUS_R
PLACE_NEAR=U1100.E44:6.35mm
LPC_CLK33M_LPCPLUS
R1959
22
PCH_CLK33M_PCIOUT
PLACE_NEAR=U1100.A40:6.35mm
PCH_CLK33M_PCIIN
System RTC Power Source & 32kHz / 25MHz Clock Generator
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.
PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)
PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary
GreenClk 25MHz Power
PP3V3_S5
SB XTAL Power
PP1V5_S0
Camera XTAL Power
PP1V2_CAM_XTALPCIEVDD
TBT XTAL Power
PP3V3_TBTLC
NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).
C1924
0.1UF
C1920
0.1UF
C1922
0.1UF
C1902
1UF
U1900
SLG3NB148CV
TQFN
CRITICAL
VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.
+V3.3A should be first available ~3.3V power to reduce VBAT draw.
SYSCLK_CLK32K_RTC
SYSCLK_CLK25M_SB
SYSCLK_CLK25M_CAMERA
SYSCLK_CLK25M_TBT
PPVRTC_G3H
For SB RTC Power
C1910
1UF
C1905
12PF
SYSCLK_CLK25M_X2
R1905
0
SYSCLK_CLK25M_X2_R
NO STUFF
R1906
1M
CRITICAL
Y1905
3.2X2.5MM-SM
25.000MHZ-20PPM-12PF-85C
C1906
12PF
SYSCLK_CLK25M_X1
NOTE: 30 PPM crystal required
PCH ME Disable Strap
PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.
PP5V_S0
R1920
100K
Q1920
DMN5L06VK-7
SOT-563
SPI_DESCRIPTOR_OVERRIDE_LS5V
PP1V5_S0
SPI_DESCRIPTOR_OVERRIDE
R1921
1K
HDA_SDOUT_R
IPD = 9-50k
SPI_DESCRIPTOR_OVERRIDE_L
SYNC_MASTER=J15_REFERENCE
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Chipset Support
Apple Inc.
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RIO SD Card Reader Support
PP3V3_S4
R2041 470K 5% 1/20W MF 201
R2040 470K 5% 1/20W MF 201
Q2040 DMN5L06VK-7 SOT-563
SMC_PME_SDCONN
SMC_PME_S4_DARK_L
PP3V3_S3
CRITICAL
U2030 TC7SZ08FEAPE SOT665
SDCONN_STATE_CHANGE_L
To/From PCH
RIO_SDCONN_STATE_CHANGE_L
From RIO Connector
C2030 0.1UF 10% 6.3V CERM-X5R 0201
LCD HPD Inverter
(Pull-Up on CPU Page)
DP_IG_A_HPD_L
LCD_HPD
Q2010 DMN32D2LFB4 DFN1006H4-3 SYM_VER_1
HDMI HPD pull-down
HDMI_HPD
R2010 100K 5% 1/20W MF 201
Platform Reset Connections
Unbuffered
PLT_RESET_L
MAKE_BASE=TRUE
R2081 33 5% 1/16W MF-LF 402
LPCPLUS_RESET_L
R2083 33 5% 1/16W MF-LF 402
SMC_LRESET_L
R2071 0 5% 1/16W MF-LF 402
PCA9557D_RESET_L
Buffered
PP3V3_S0
CRITICAL
U2080 MC74VHC1G08 SC70-HF
PLT_RST_BUF_L
C2080 0.1UF 20% 10V CERM 402
R2080 100K 5% 1/16W MF-LF 402
R2085 0 5% 1/16W MF-LF 402
SSD_RESET_L
R2091 0 5% 1/16W MF-LF 402
CAM_PCIE_RESET_L
R2088 0 5% 1/16W MF-LF 402
AP_RESET_L
R2087 0 5% 1/16W MF-LF 402
TBT_PCIE_RESET_L
Flexible I/O Aliases
SD Card Reader is always USB3 in this implementaton.
USB3_SD_D2R_P
USB3_SD_D2R_N
USB3_SD_R2D_C_P
USB3_SD_R2D_C_N
Flexible I/O Configuration Strap
Must pull signal correctly even if always USB or PCIe
PP3V3_S0
R2030 100K 5% 1/20W MF 201
SD_SEL_PCIE_L_USB_H
RAM Configuration Straps
MLB_RAMCFG3
MLB_RAMCFG2
XDP_DD1_MLB_RAMCFG1
MLB_RAMCFG0
RAMCFG0:L R2002 1K 5% 1/20W MF 201
RAMCFG1:L R2011 1K 5% 1/20W MF 201
RAMCFG2:L R2012 1K 5% 1/20W MF 201
RAMCFG3:L R2013 1K 5% 1/20W MF 201
Redwood Ridge Support
RR output is open-drain, no isolation necessary
PP3V3_S0
R2075 10K 5% 1/20W MF 201
TBT_CIO_PLUG_EVENT_L
MAKE_BASE=TRUE
GPIO Glitch Prevention
PP3V3_S0
CRITICAL
U2000 SOT833 74AUP2G08GT/S505
C2013 0.1UF 10% 16V X5R-CERM 0201
TBT_PWR_EN must be high for JTAG Programming
TBT_PWR_EN
JTAG_ISP_TCK
TBT_PWR_EN_PCH
LPC_PWRDWN_L
JTAG_TBT_TCK
TBT_PWR_EN
Redwood Ridge JTAG Isolation
TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V
PP3V3_TBTLC
PP3V3_S0
C2060 0.1UF 10% 16V X5R-CERM 0201
R2061 10K 5% 1/20W MF 201
R2062 10K 5% 1/20W MF 201
R2063 10K 5% 1/20W MF 201
Pull-up values TBD
U2060 SN74AUP3G07DQER X2SON
JTAG_TBT_TMS_PCH
JTAG_ISP_TDO
JTAG_ISP_TDI
JTAG_TBT_TMS
JTAG_TBT_TDO
JTAG_TBT_TDI
To/From PCH
(Pull-ups on PCH page)
To/From RR
CRITICAL
GS3 Connector Support
DEVSLP not supported on LPT-H
SSD_DEVSLP
R2070 10K 5% 1/20W MF 201
SYNC_MASTER=J15_REFERENCE
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PAGE TITLE
Project Chipset Support
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REVISION <E4LABEL>
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

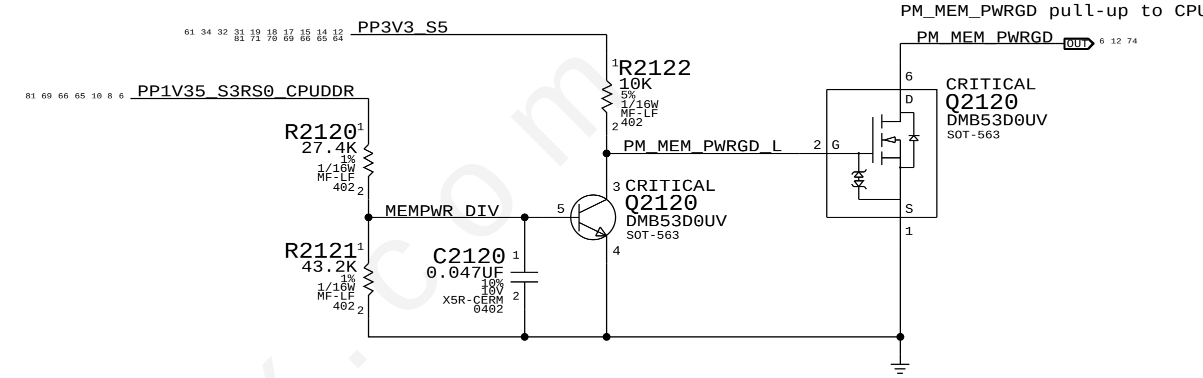
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



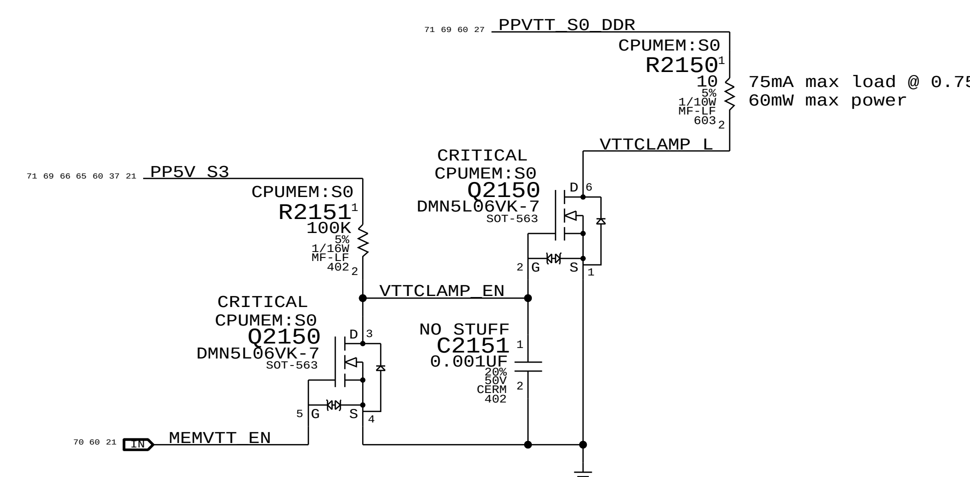
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



S0 to S3 to S0

Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
1	0	1	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

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PAGE TITLE: CPU Memory S3 Support

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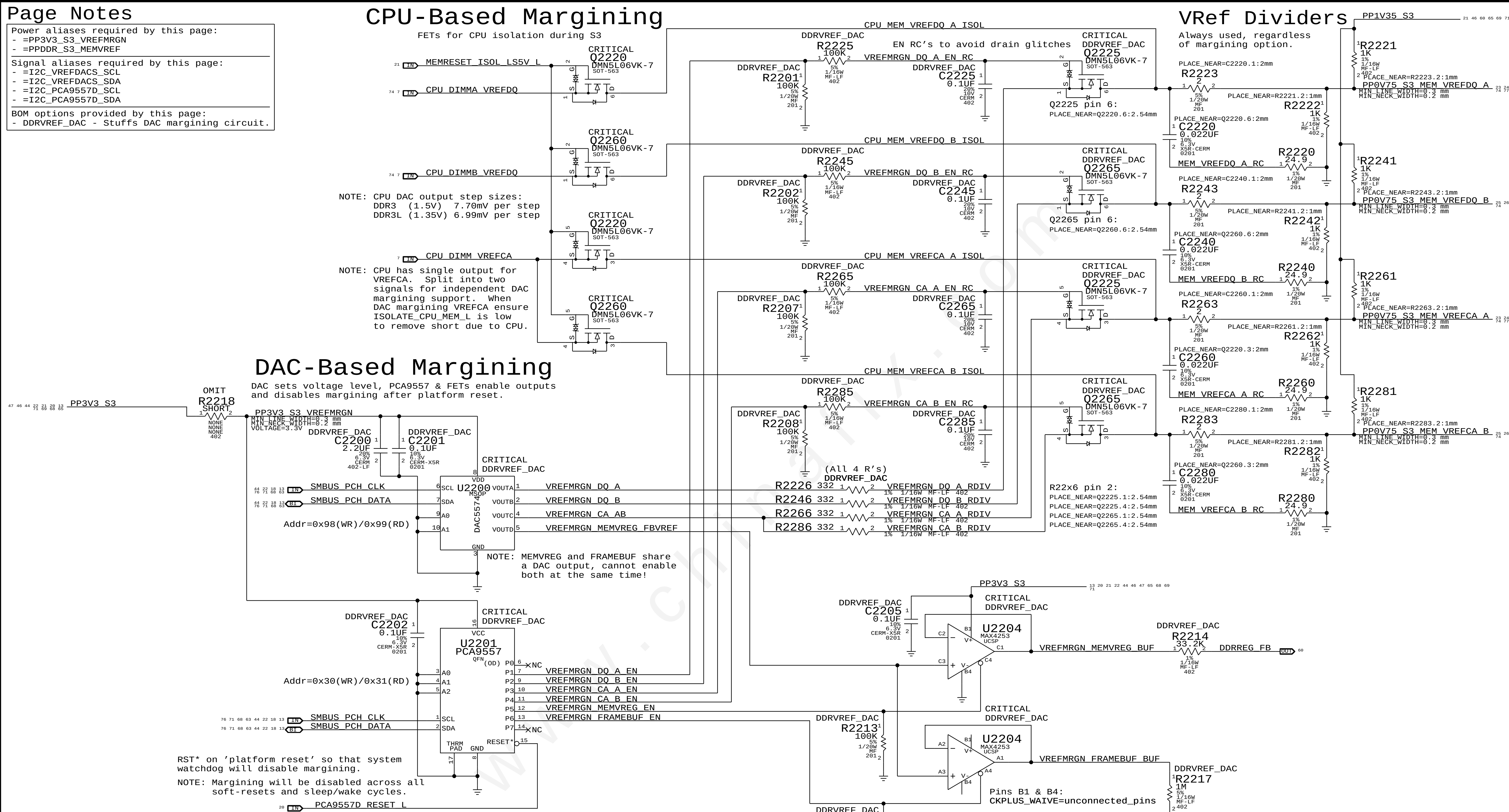
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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5

	DDR3 (1.5V)	DDR3L (1.35V)	DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)	0.675V (DAC: 0x34 = 0.670mV)	1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)	0.275V - 1.075V (+/- 400mV)	1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)	0.000V - 1.354V (0x00 - 0x69)	0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)	0.269V - 1.083V (+/- 406mV)	1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)	+811uA - -816uA (- = sourced)	+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output	7.67mV / step @ output	2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

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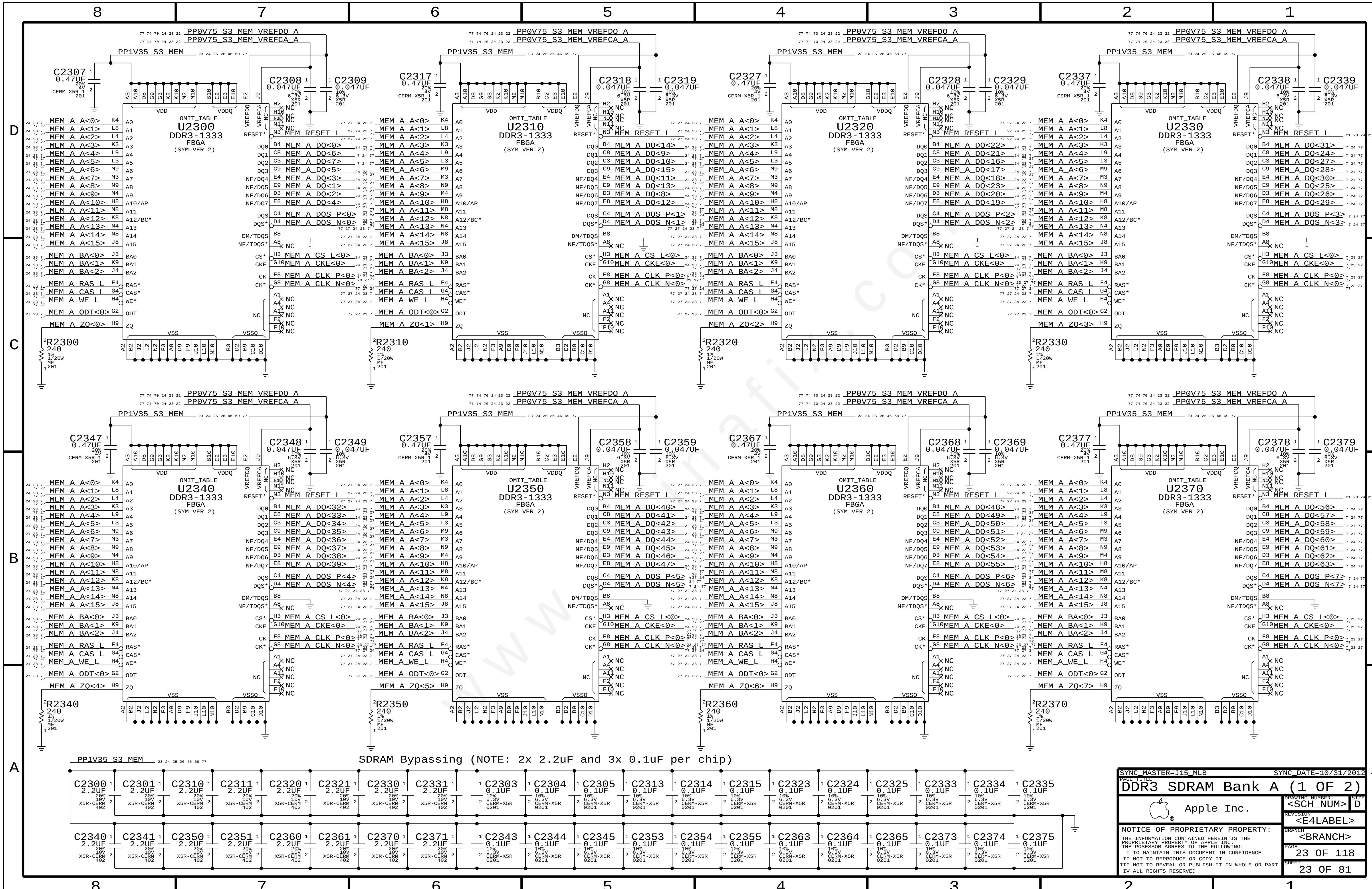
PAGE TITLE: DDR3 VREF MARGINING

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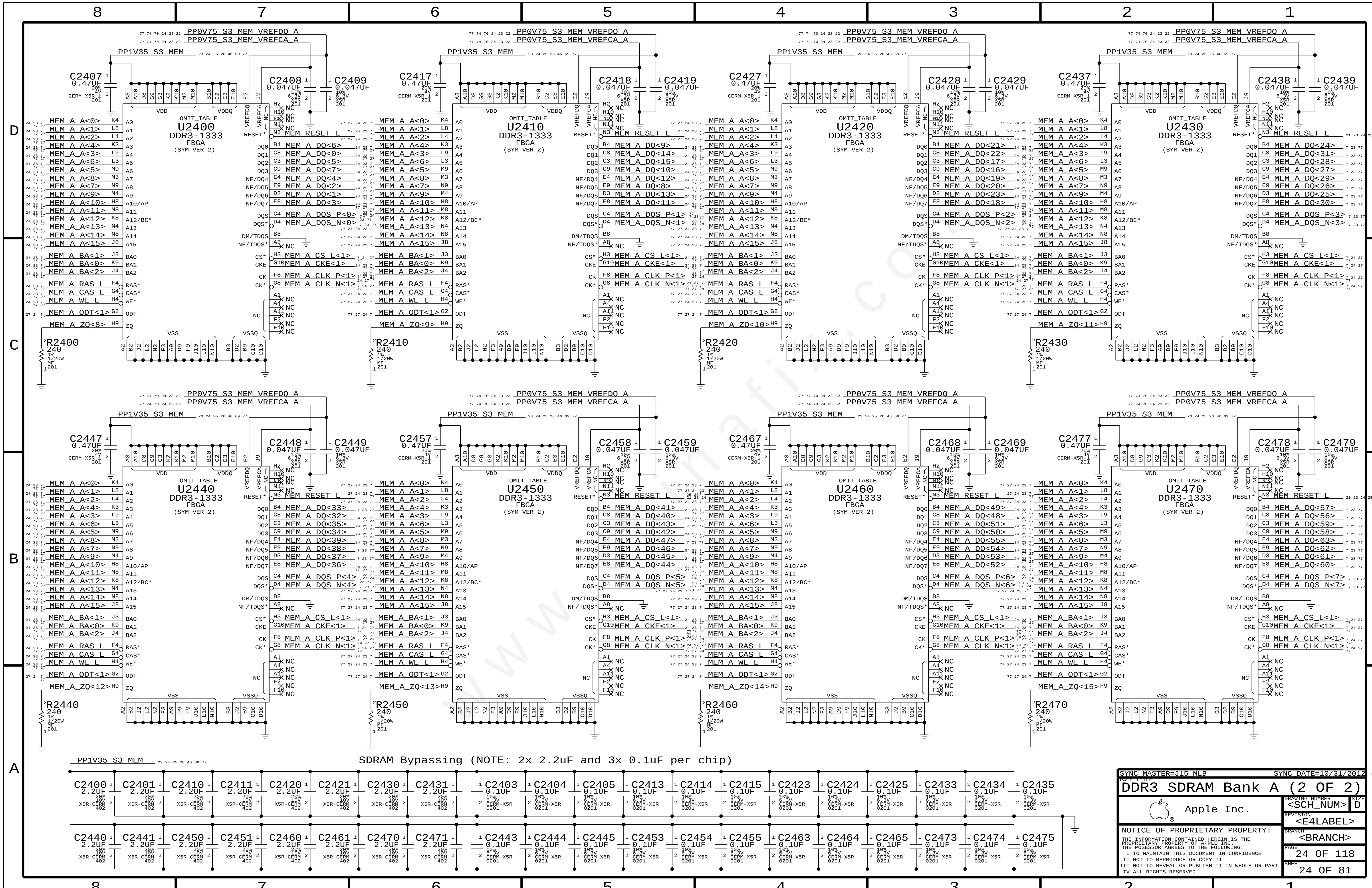
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U2300 DDR3-1333 FBGA (SYM VER 2)
U2310 DDR3-1333 FBGA (SYM VER 2)
U2320 DDR3-1333 FBGA (SYM VER 2)
U2330 DDR3-1333 FBGA (SYM VER 2)
U2340 DDR3-1333 FBGA (SYM VER 2)
U2350 DDR3-1333 FBGA (SYM VER 2)
U2360 DDR3-1333 FBGA (SYM VER 2)
U2370 DDR3-1333 FBGA (SYM VER 2)
PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
PP1V35_S3_MEM
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
DDR3 SDRAM Bank A (1 OF 2)
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DDR3 SDRAM Bank A (2 OF 2)

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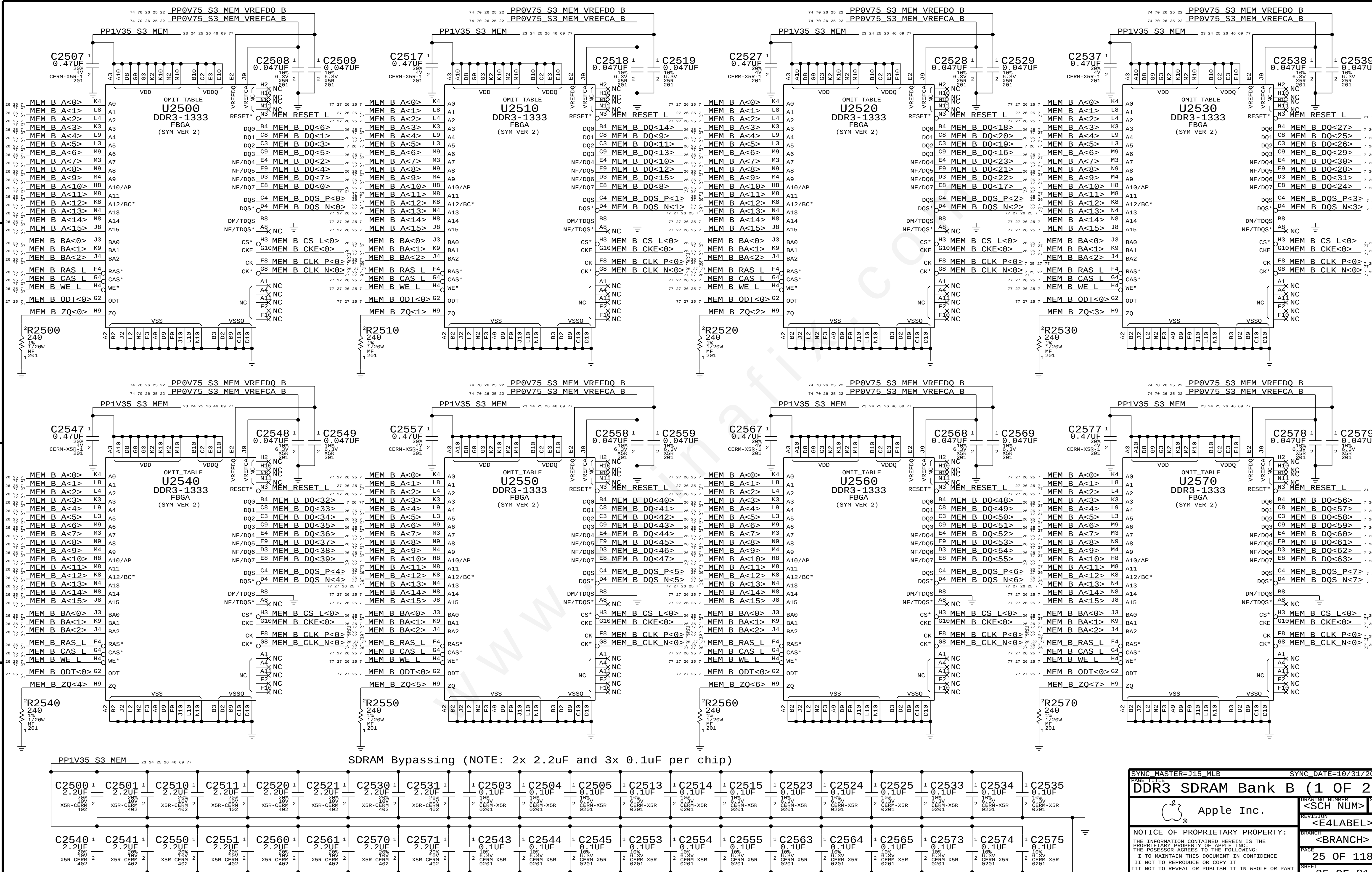
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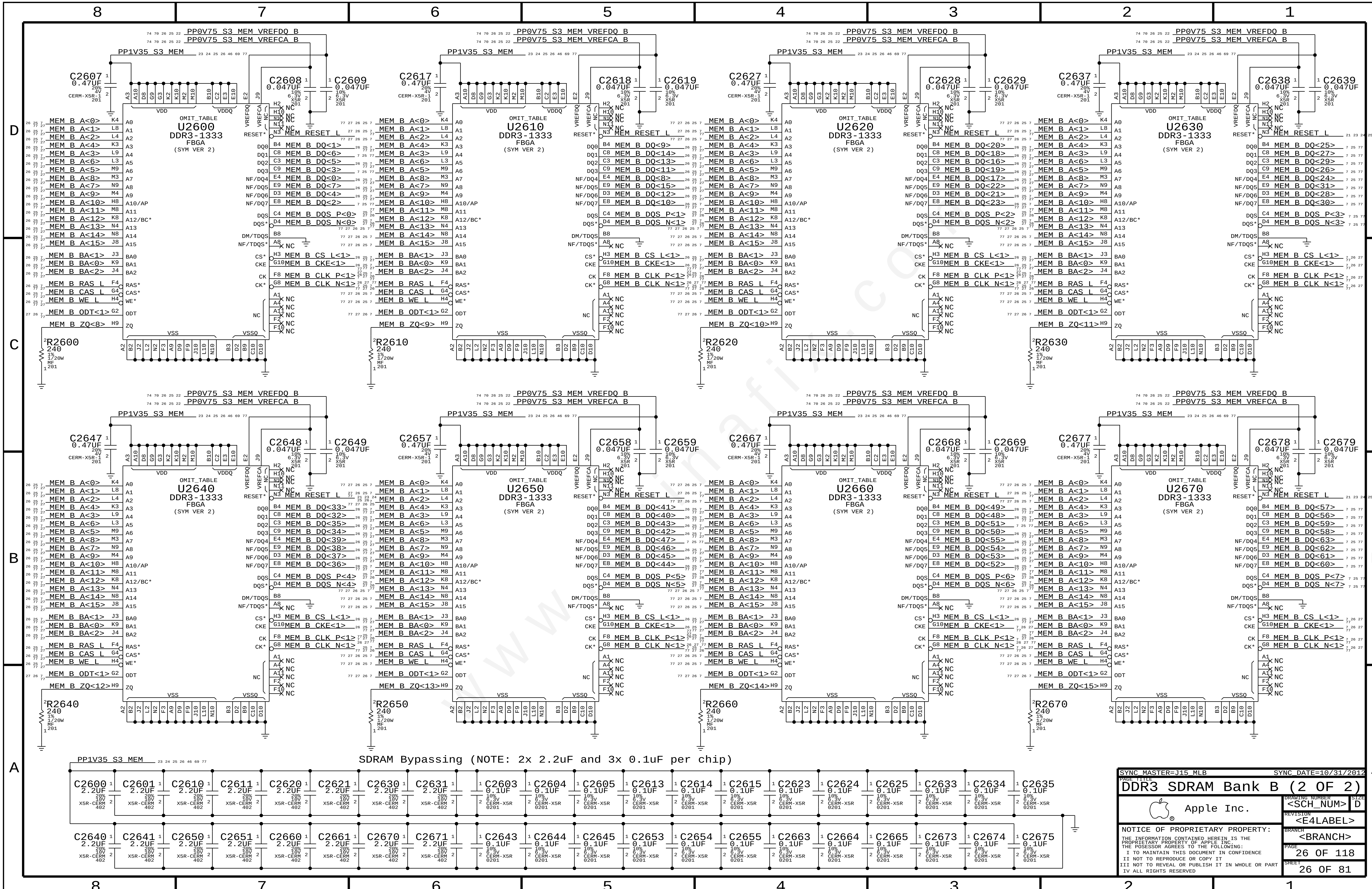
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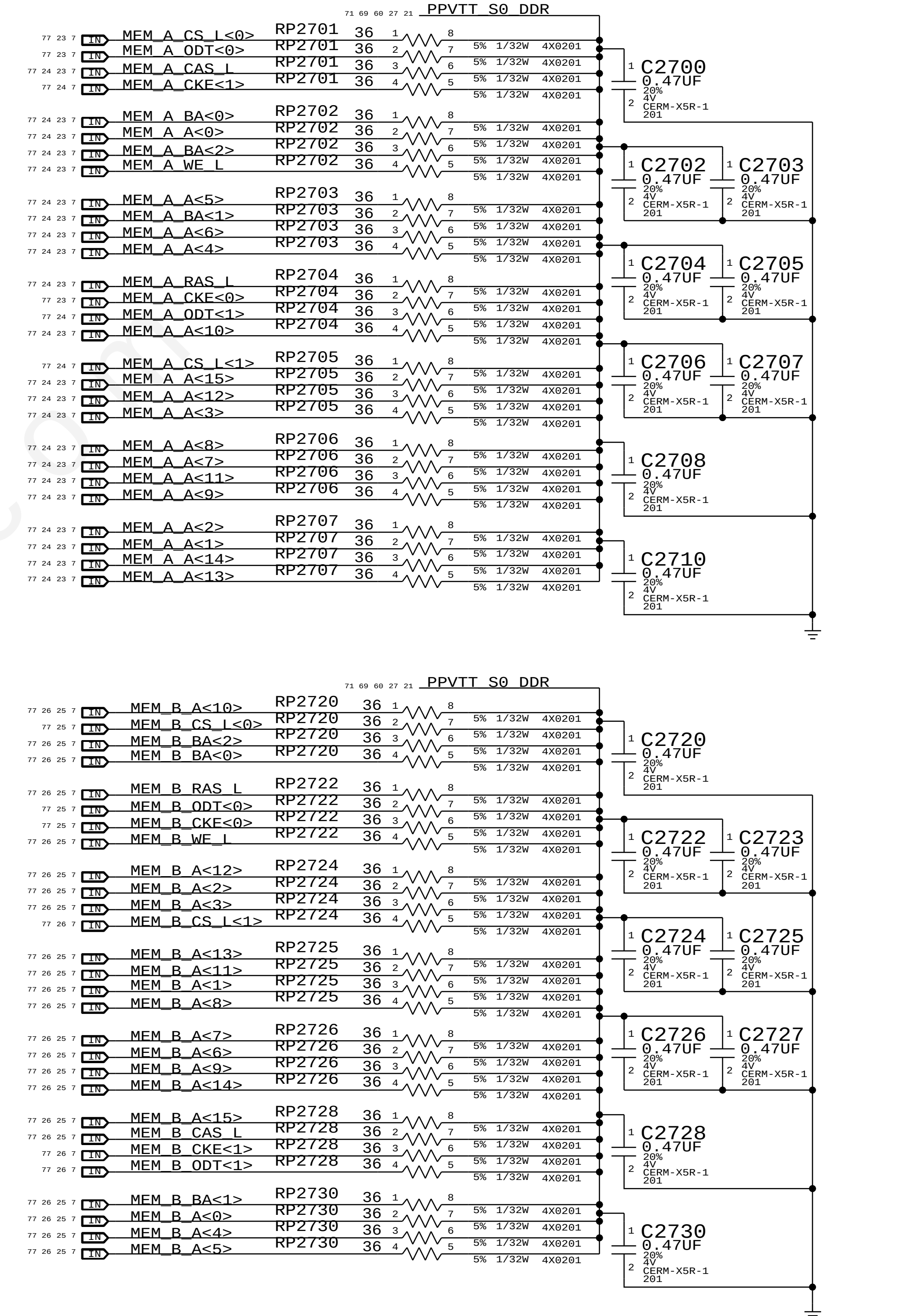
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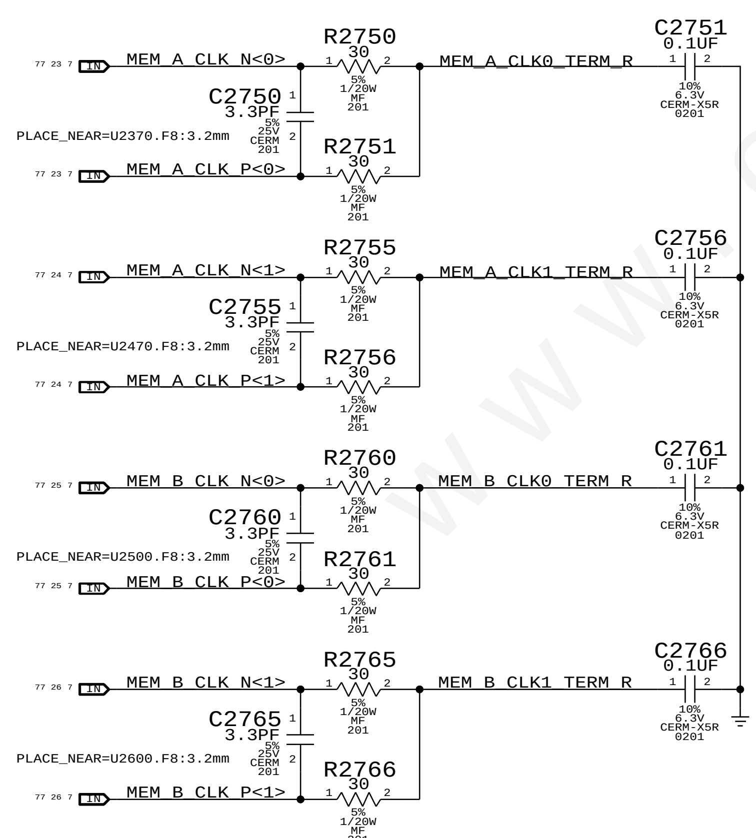
PP0V75_S3_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFCA_B
PP1V35_S3_MEM
U2600
U2610
U2620
U2630
U2640
U2650
U2660
U2670
OMIT_TABLE
DDR3-1333
FBGA
(SYM VER 2)
VDD
VDDQ
VSS
VSSQ
VREFDQ
VREFCA
RESET*
MEM_B_RESET_L
MEM_B_CS_L<1>
MEM_B_CKE<1>
MEM_B_CLK_P<1>
MEM_B_CLK_N<1>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<1>
MEM_B_ZQ<8>
MEM_B_ZQ<9>
MEM_B_ZQ<10>
MEM_B_ZQ<11>
MEM_B_ZQ<12>
MEM_B_ZQ<13>
MEM_B_ZQ<14>
MEM_B_ZQ<15>
R2600
R2610
R2620
R2630
R2640
R2650
R2660
R2670
240
1%
1/20W
MF
201
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
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DDR3 SDRAM Bank B (2 OF 2)
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<BRANCH>
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JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

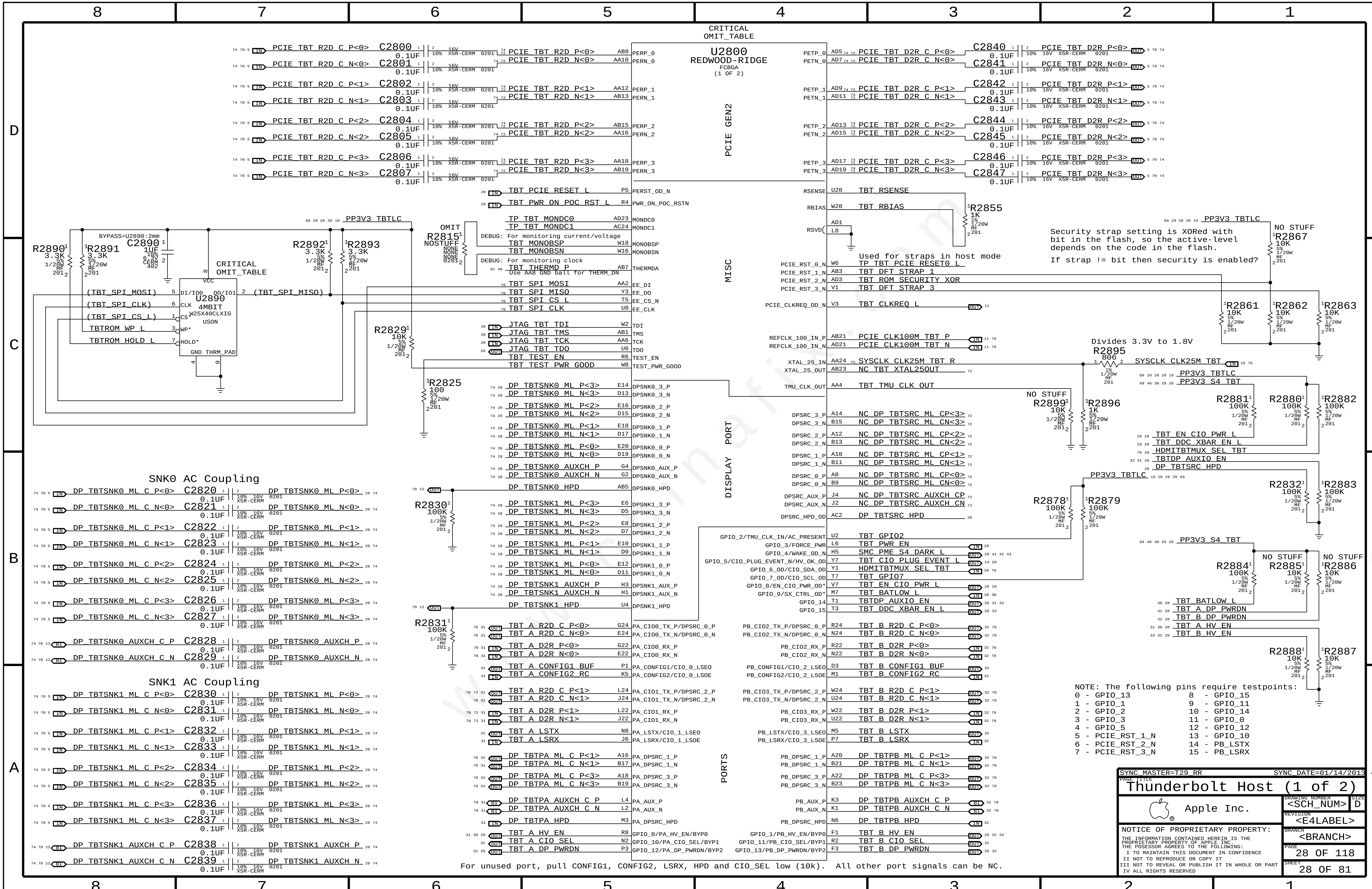
DDR3 Termination

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

SYNC_MASTER=T29_RR SYNC_DATE=01/14/2013

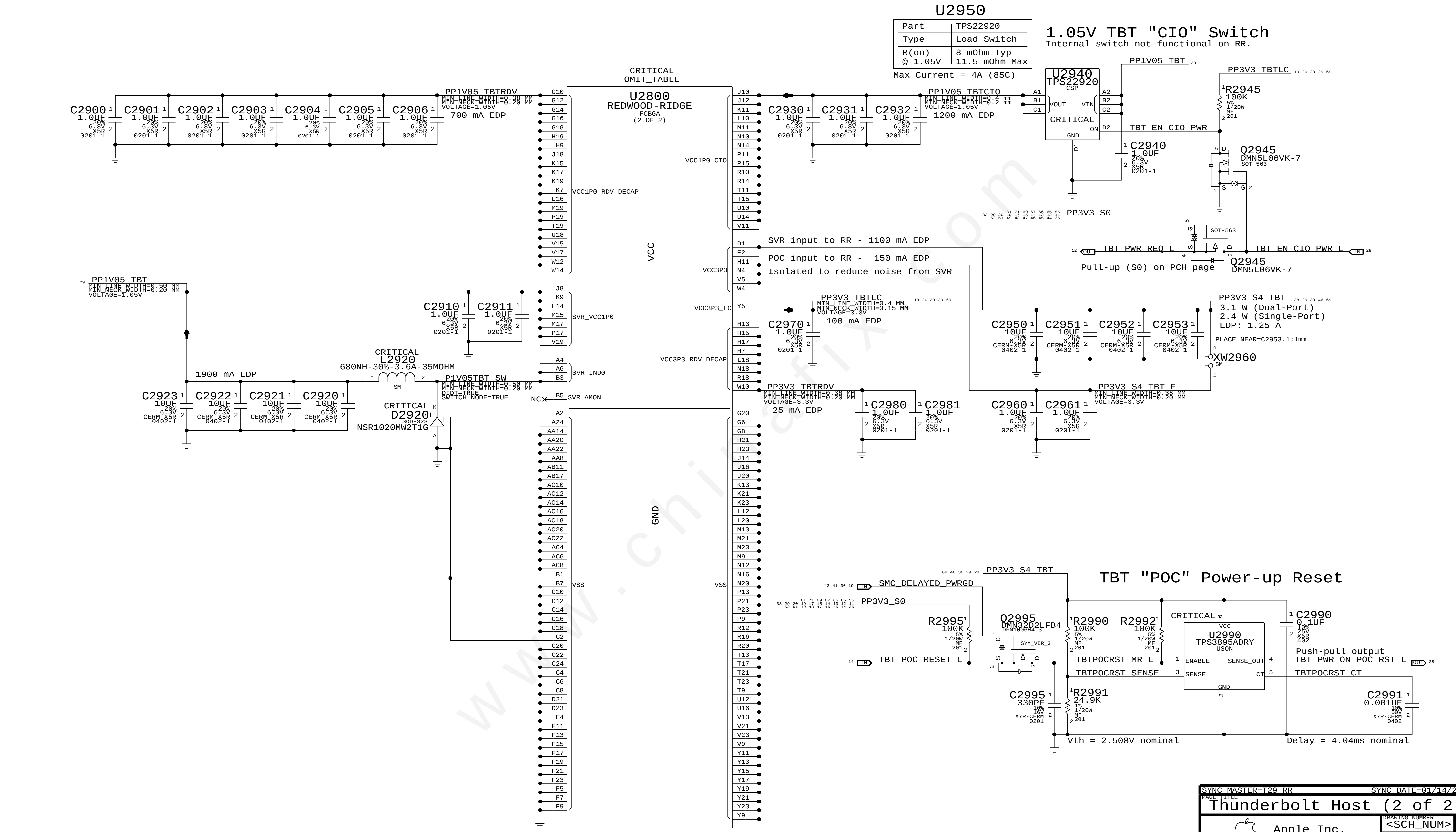
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Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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PAGE TITLE: Thunderbolt Host (2 of 2)

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REVISION: <E4LABEL>

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EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

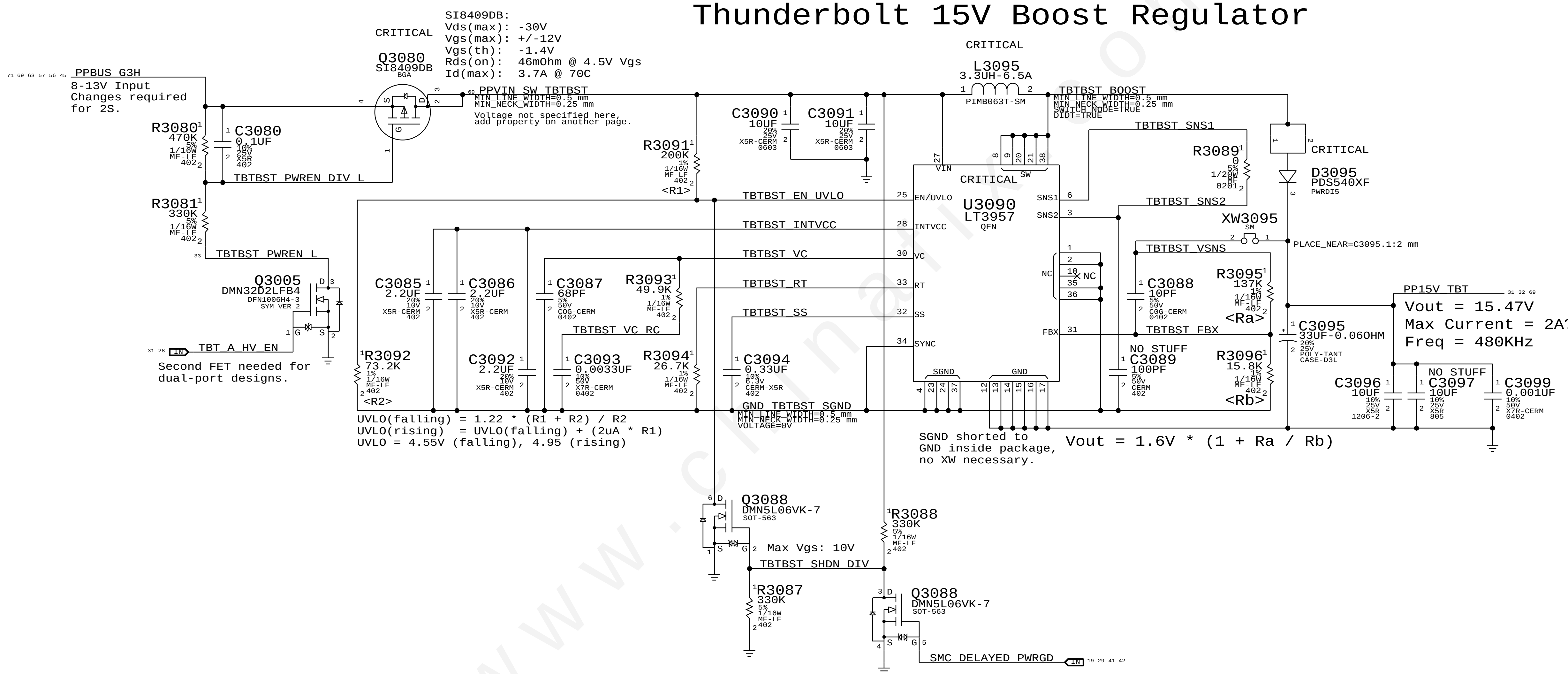
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

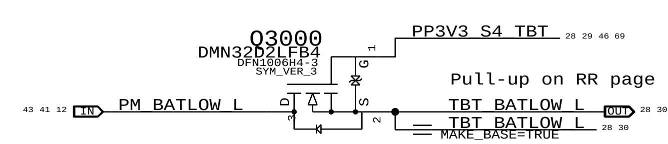
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator



BATLOW# Isolation



SYNC_MASTER=T29_RR SYNC_DATE=01/14/2013

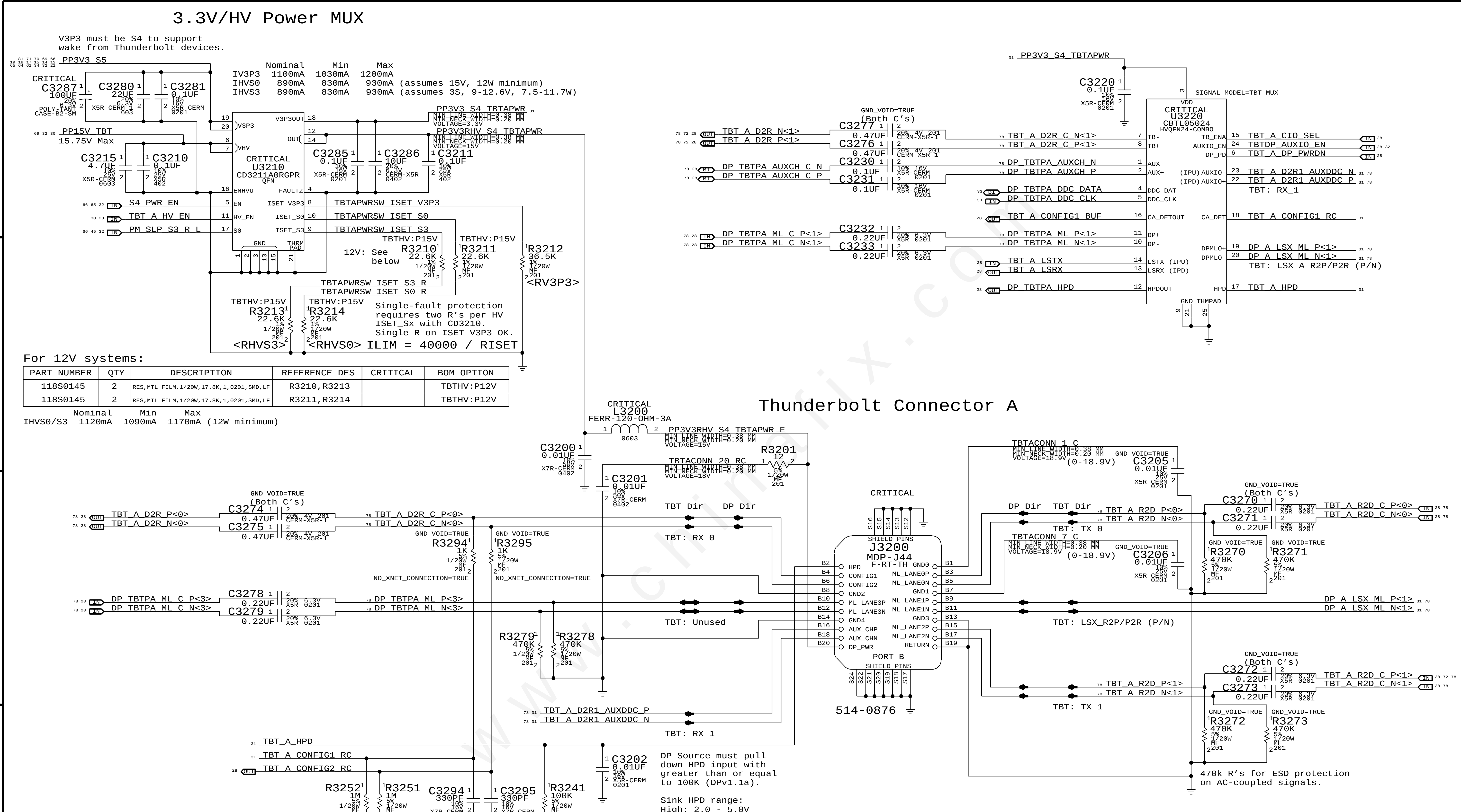
PAGE TITLE: Thunderbolt Mobile Support

DRAWING NUMBER: <SCH_NUM> SIZE: D

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE
Thunderbolt Connector A

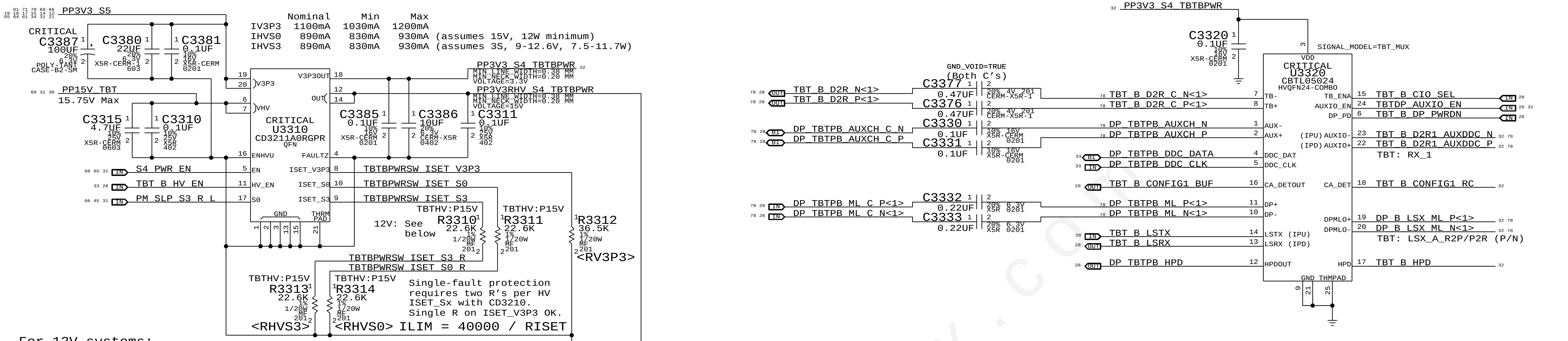
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3.3V/HV Power MUX

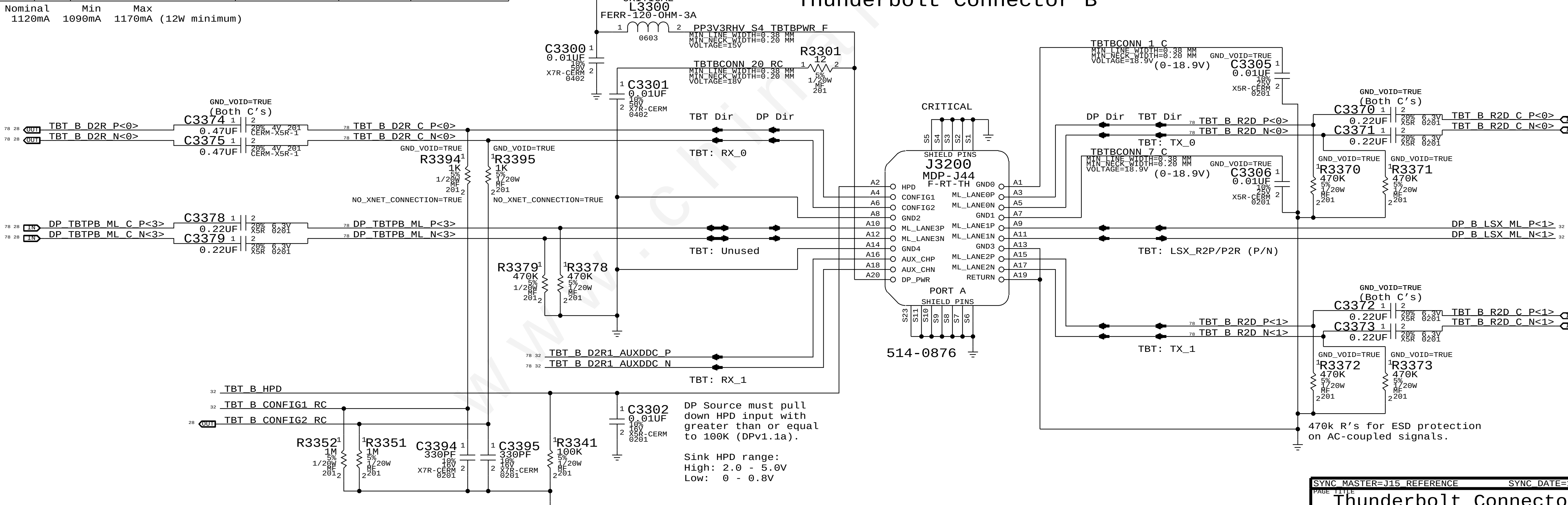


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

Thunderbolt Connector B



SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

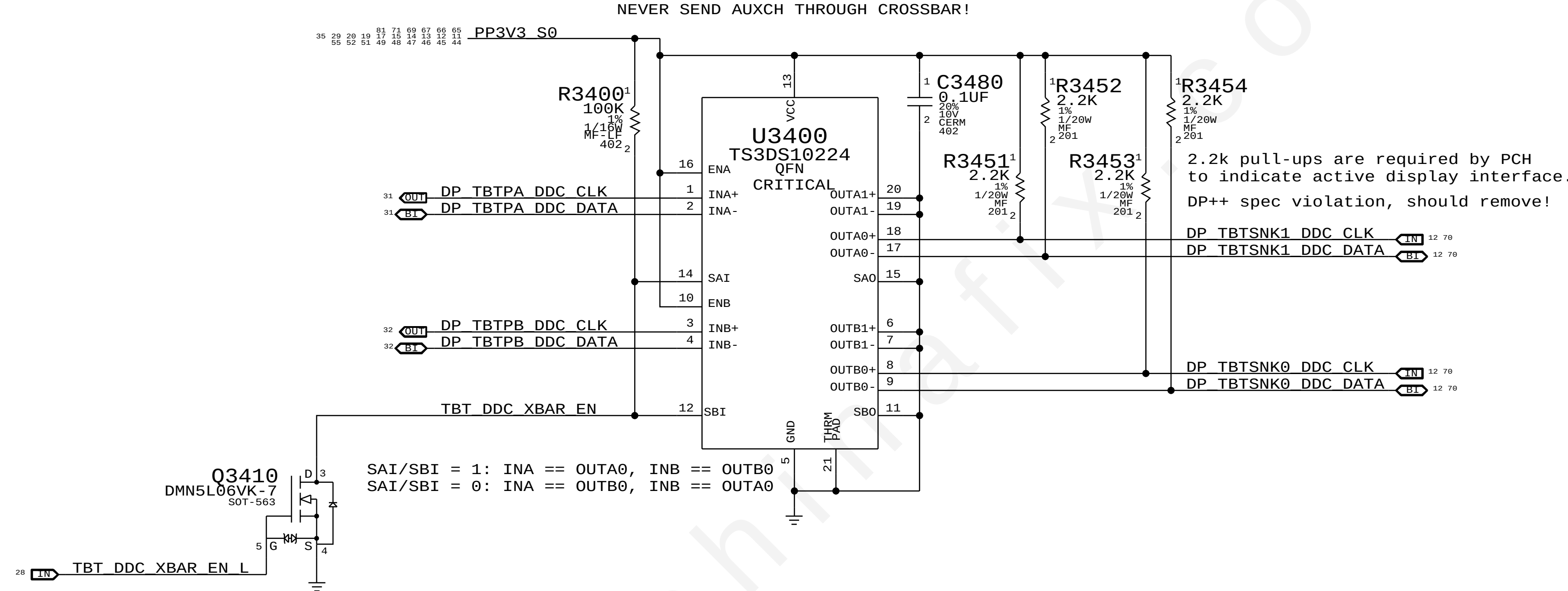
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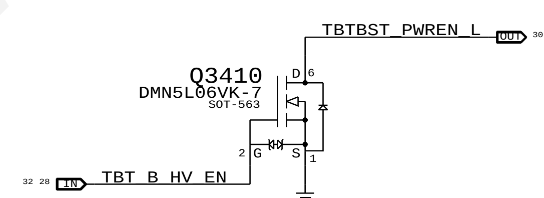
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DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!



Second TBT Port HV Boost Enable



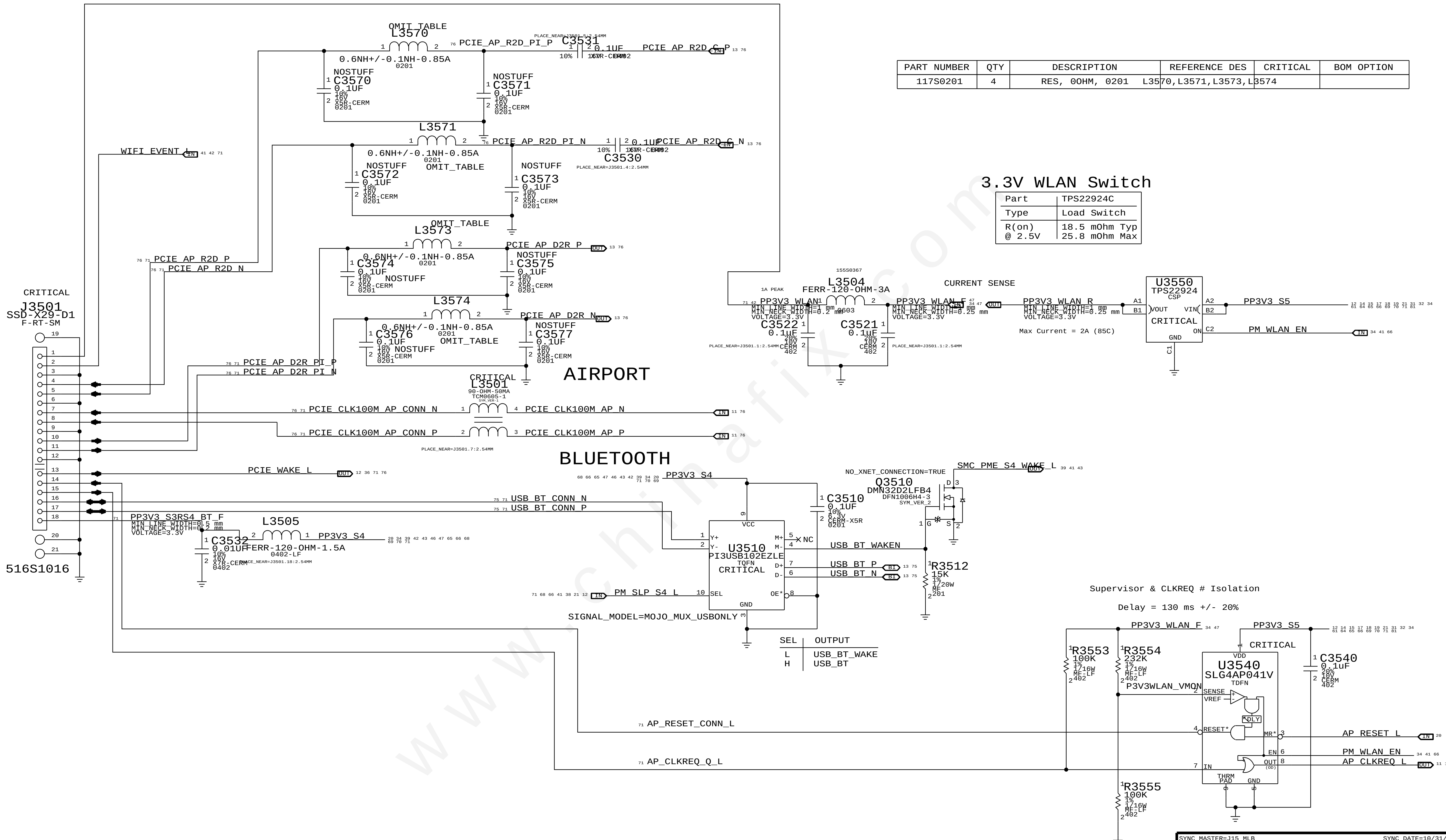
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DDC Crossbar

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		

3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

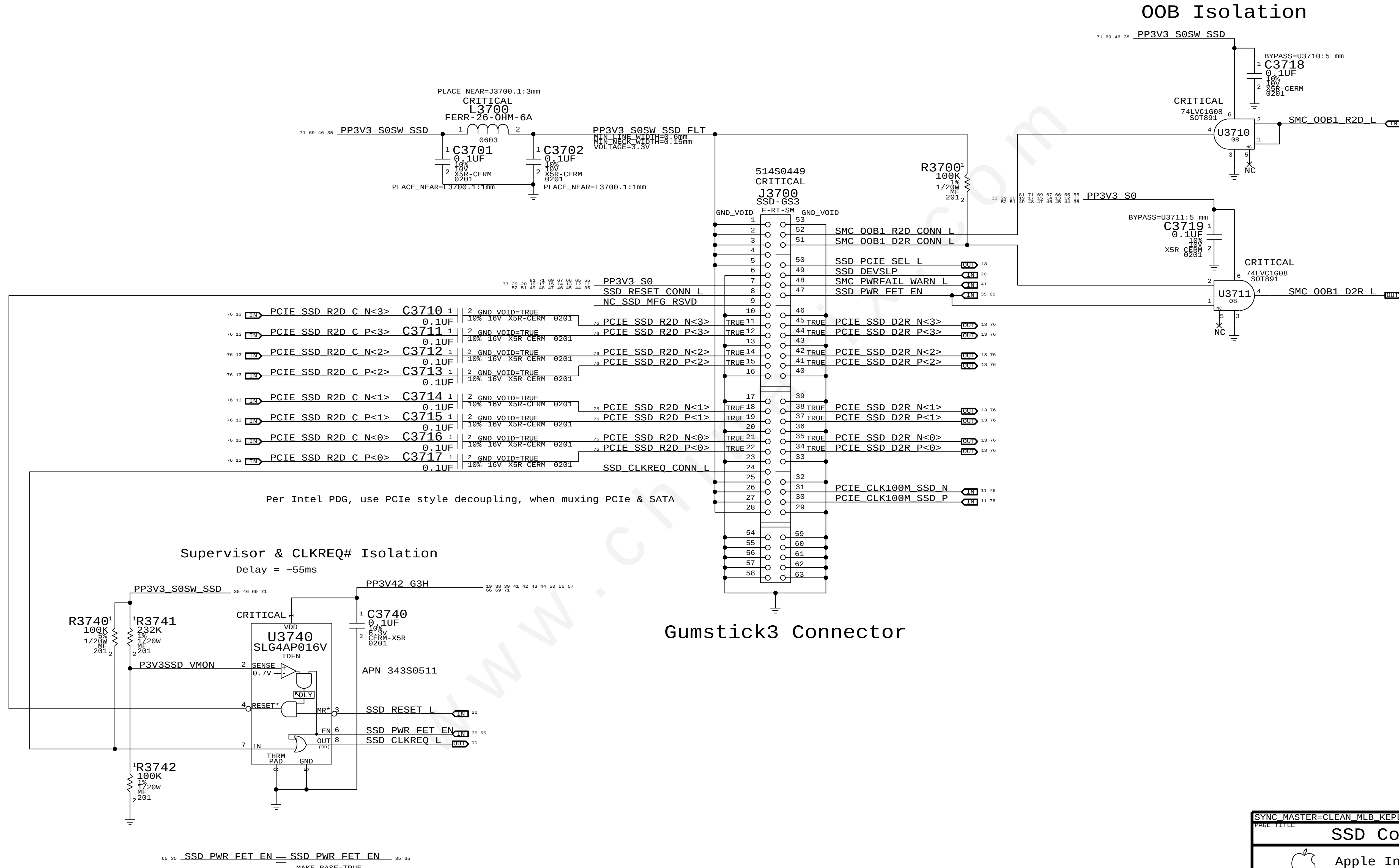
X29C CONNECTOR

Apple Inc.

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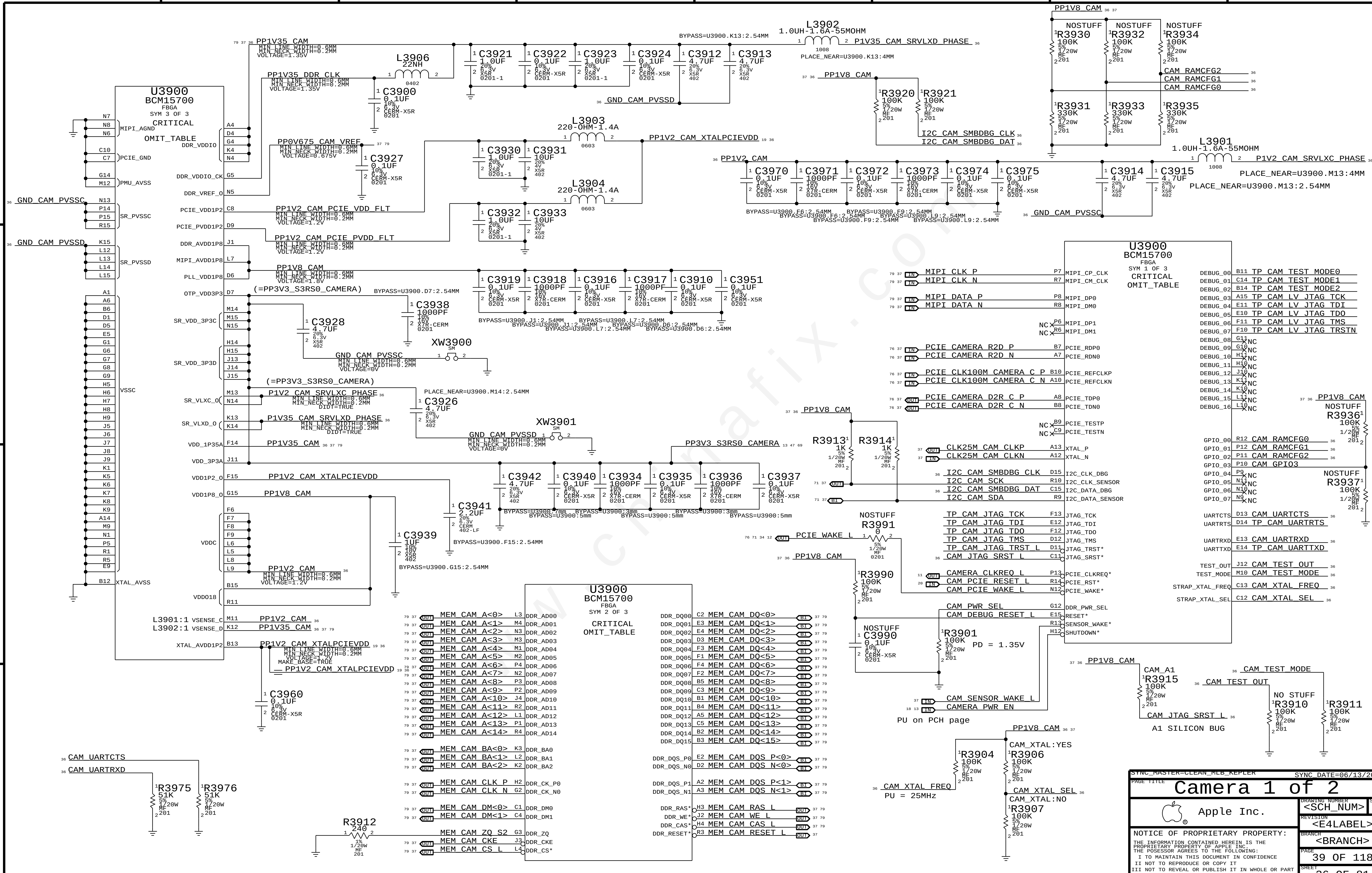
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PAGE TITLE

SSD Connector

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SYNC_MASTER=CLEAN_MLB_KEPLER SYNC_DATE=06/13/2013

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Camera 1 of 2

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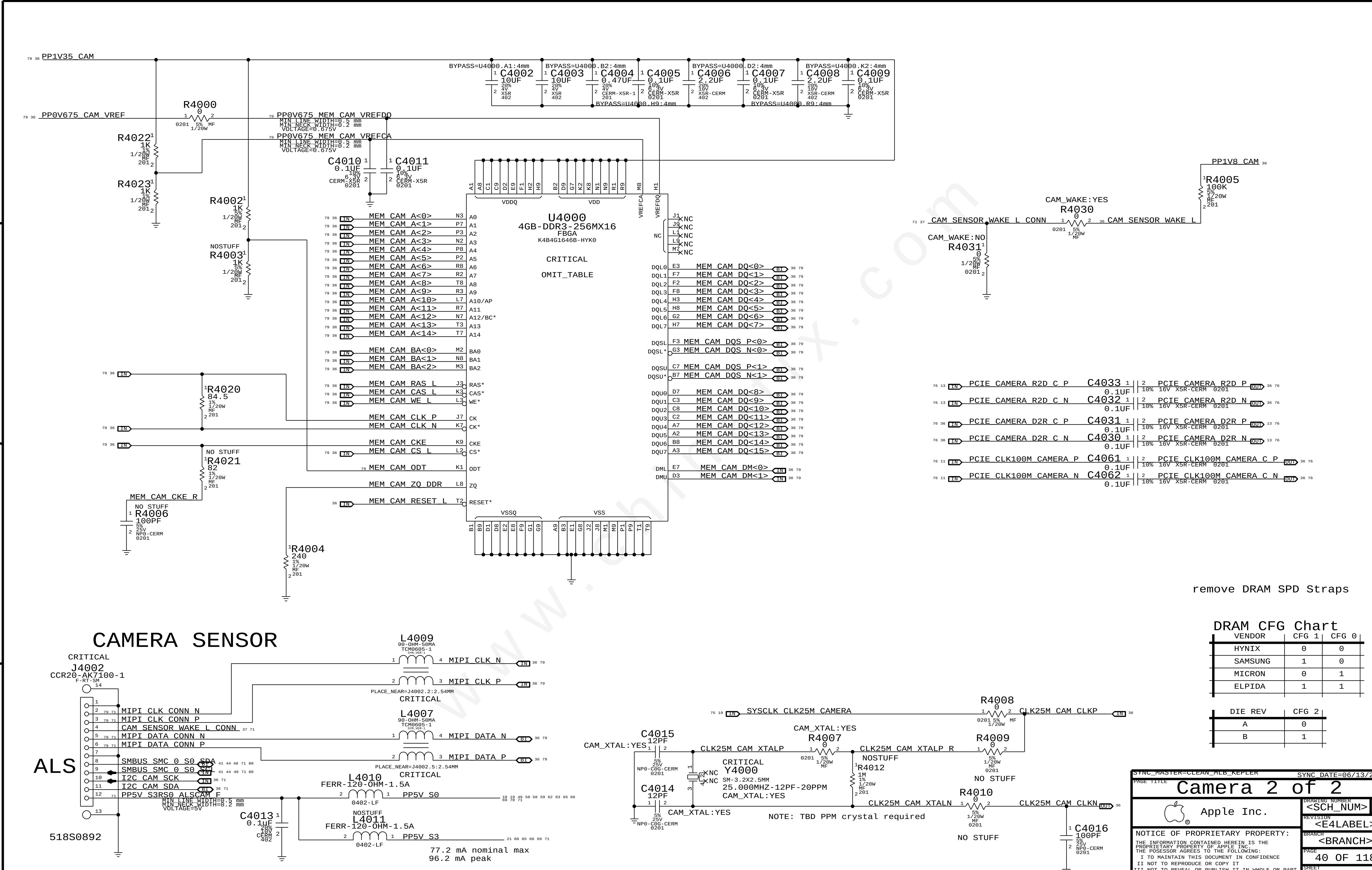
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DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

SYNC_MASTER=CLEAN_MLB_KEPLER SYNC_DATE=06/13/2013

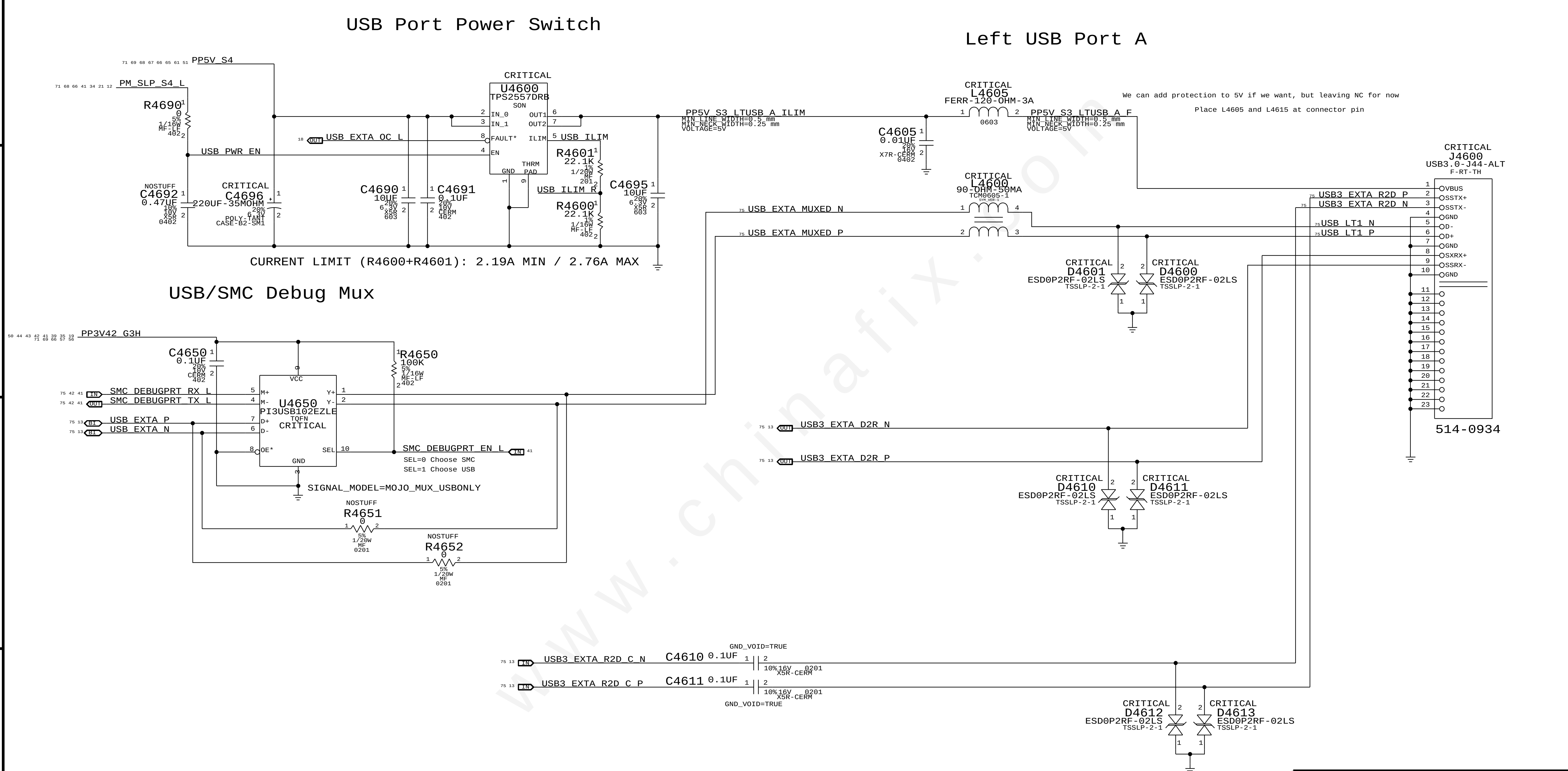
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Apple Inc.

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USB 3.0 CONNECTORS

DRAWING NUMBER <SCH_NUM> SIZE D

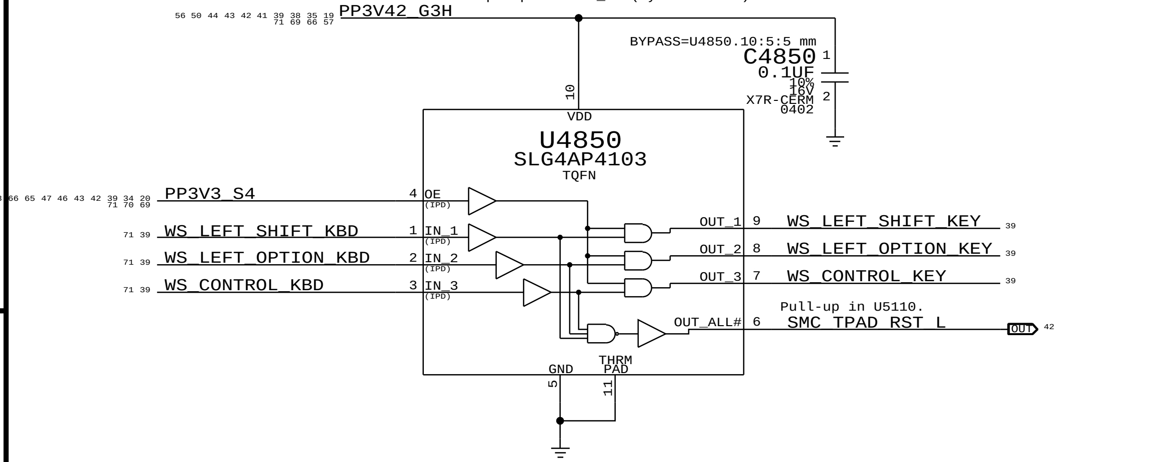
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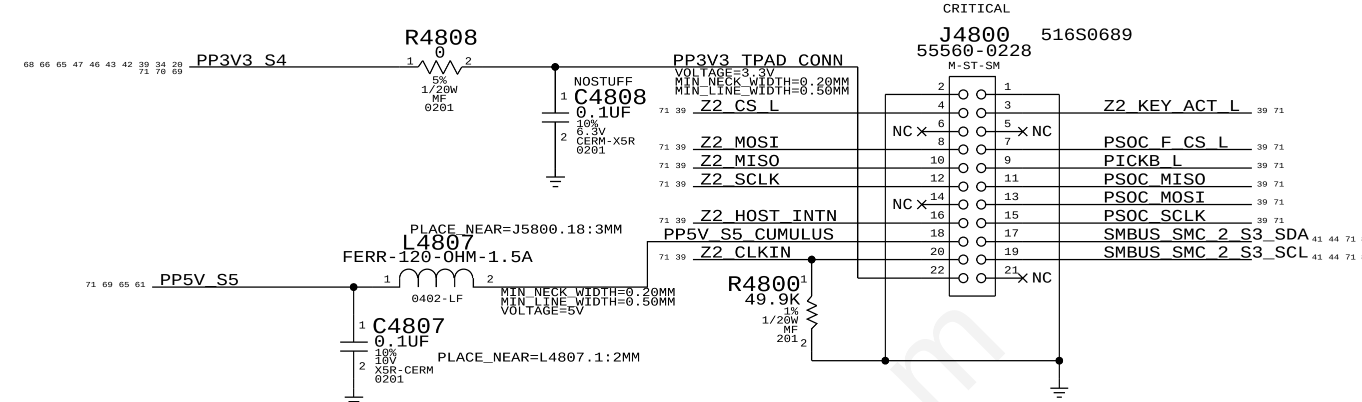
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SMC Manual Reset & Isolation

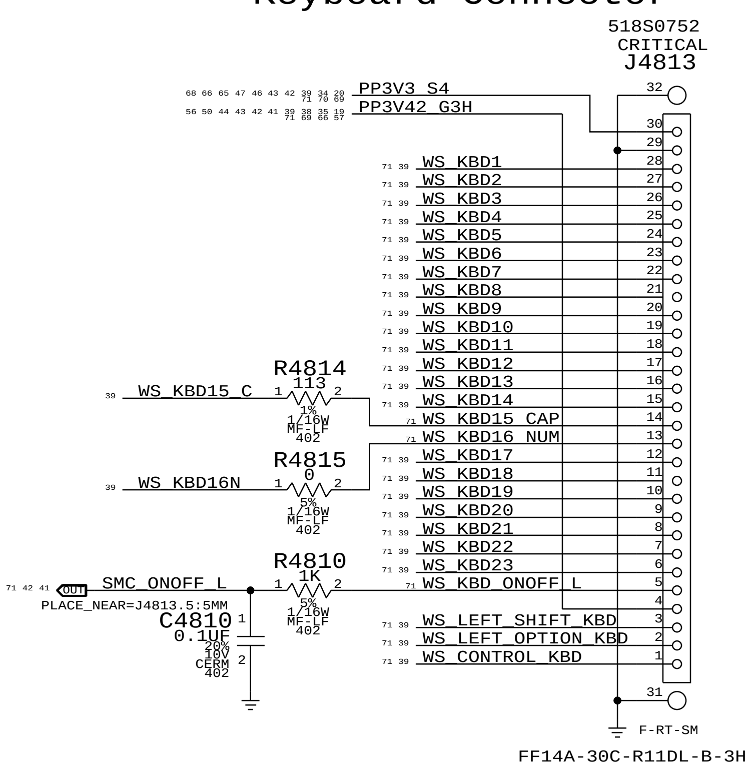
Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).



IPD Flex Connector

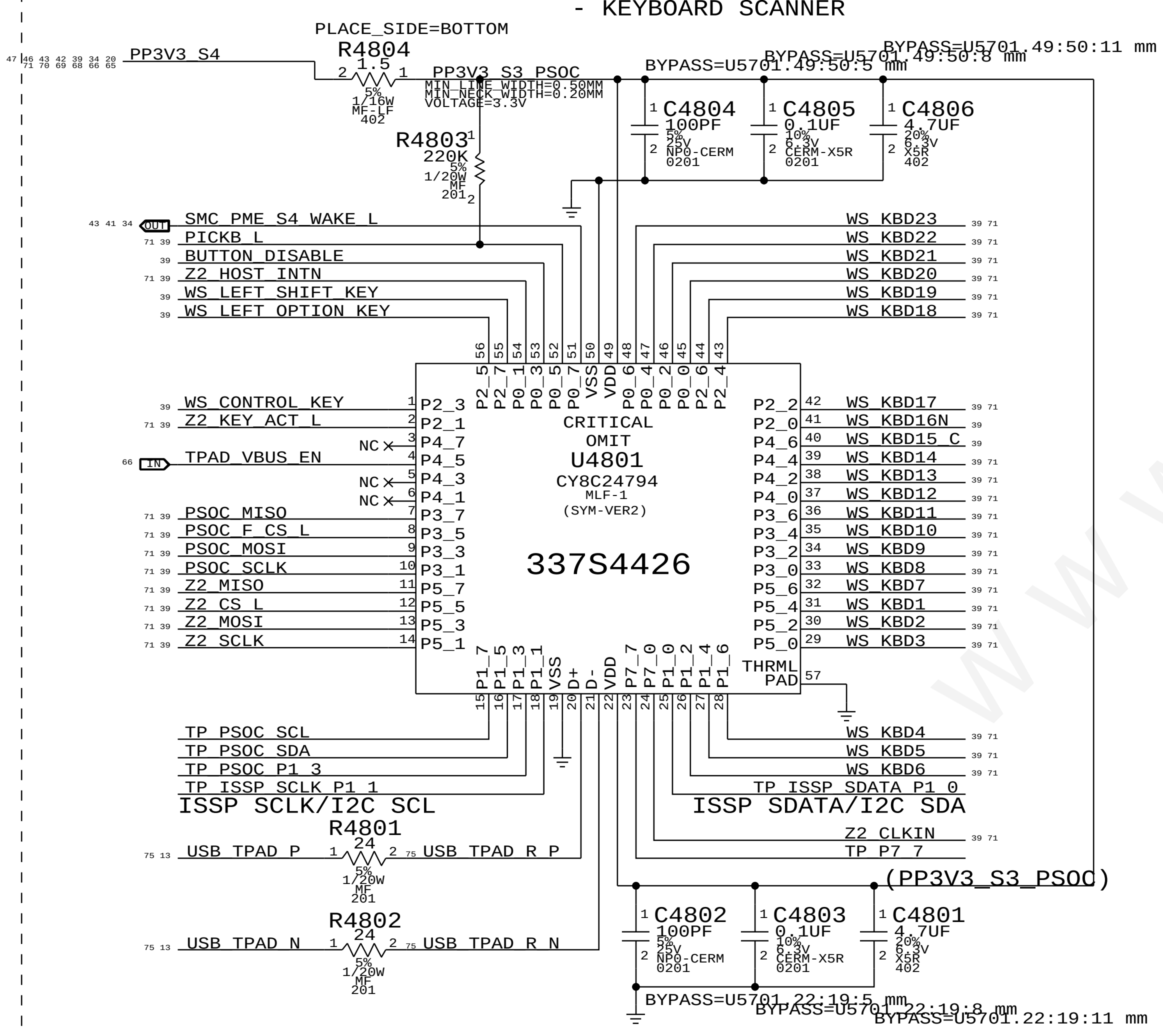


Keyboard Connector



PSOC USB CONTROLLER

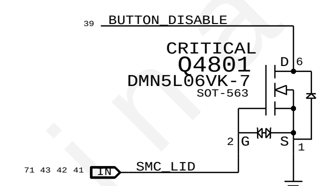
- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

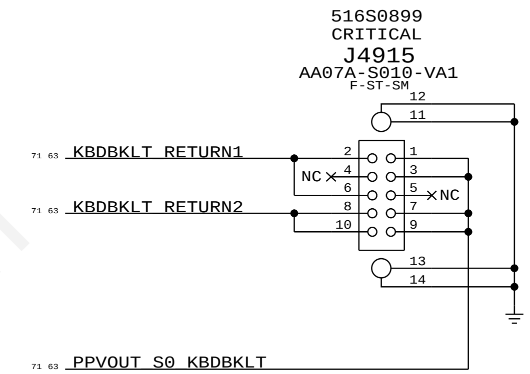
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PAGE TITLE
KEYBOARD/TRACKPAD (1 OF 2)

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Keyboard Backlight Connector



SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE: KEYBOARD/TRACKPAD (2 OF 2)

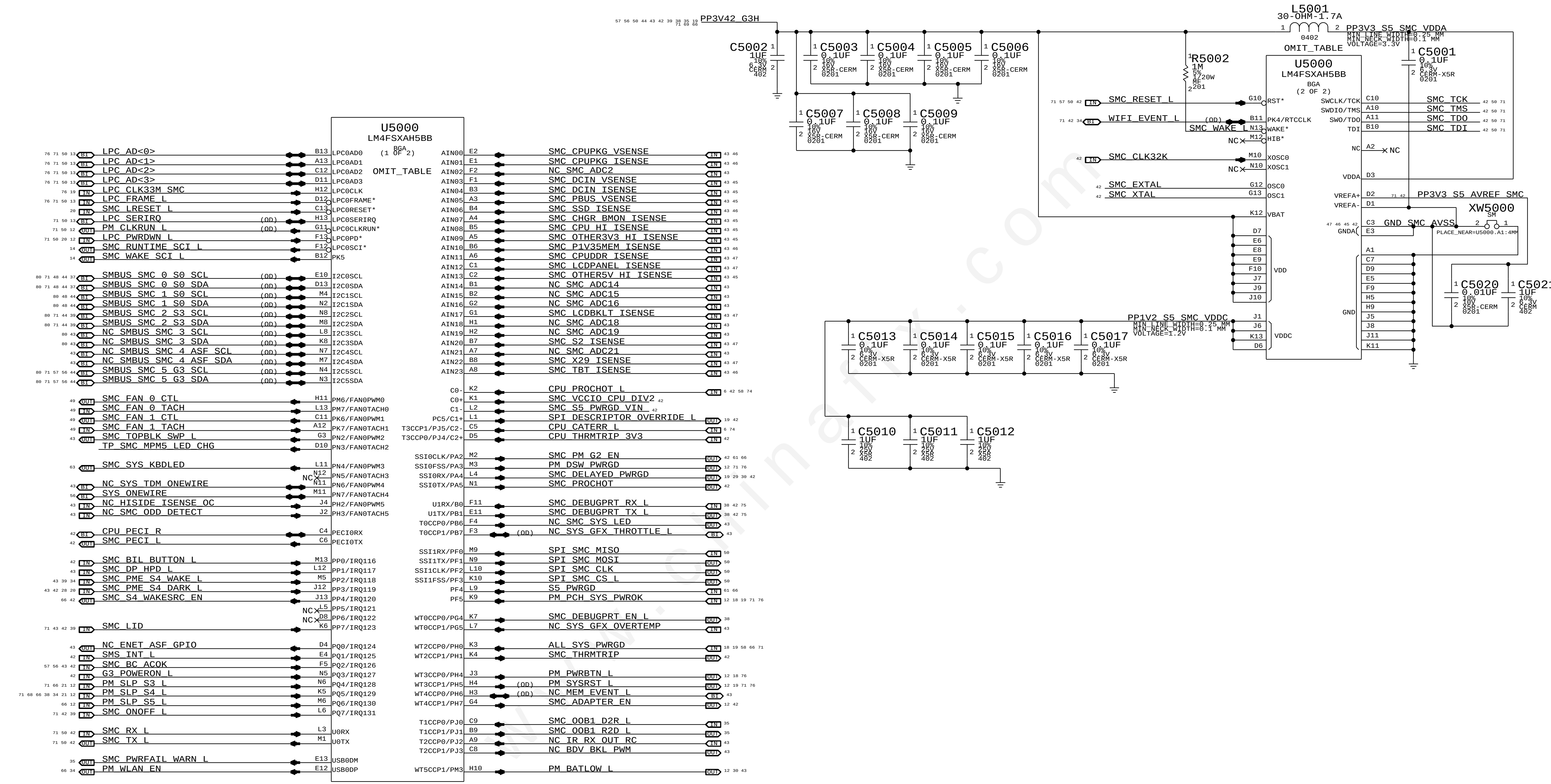
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DRAWING NUMBER: <SCH_NUM> SIZE: D

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BRANCH: <BRANCH>

NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

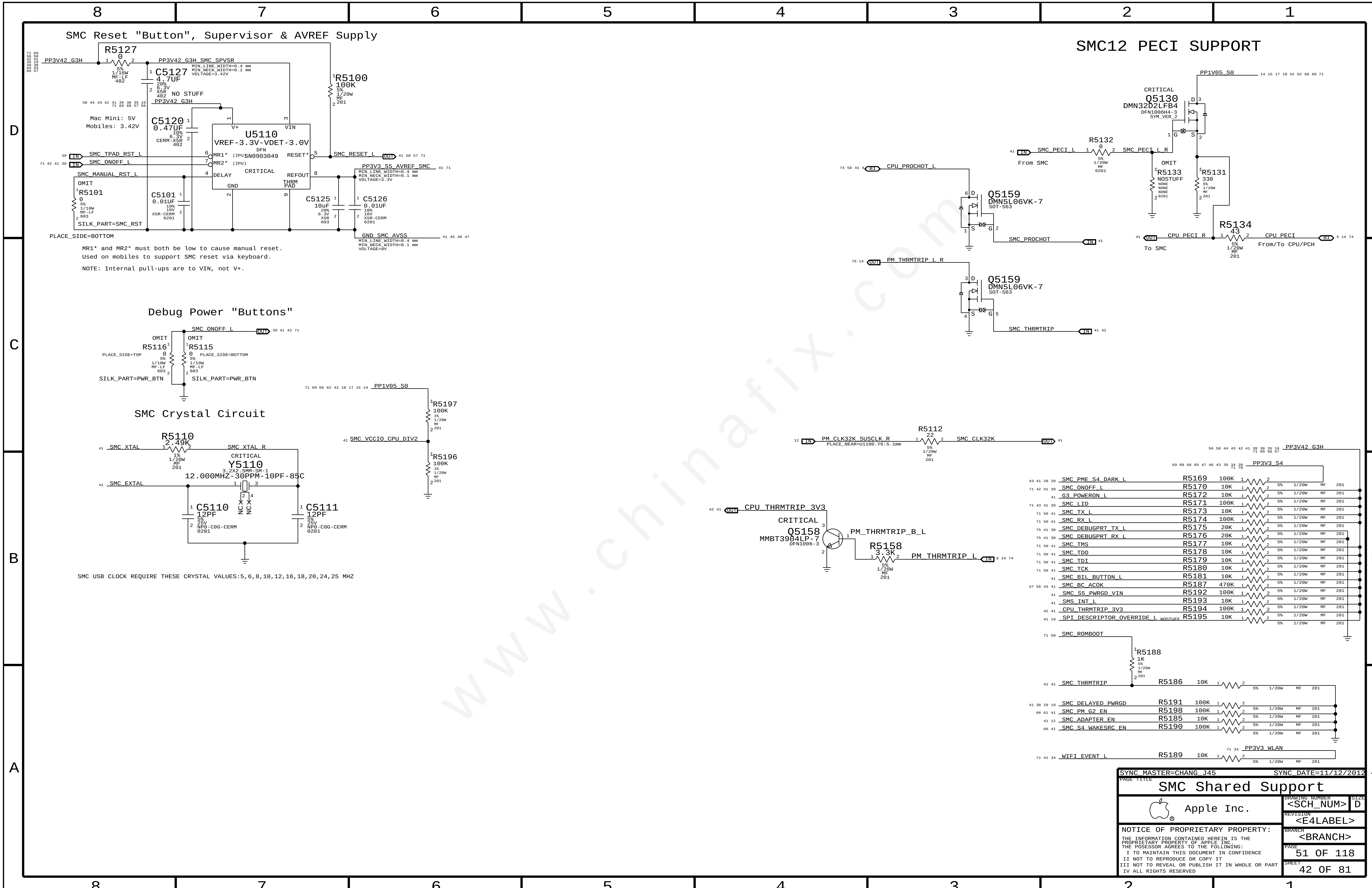
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SMC

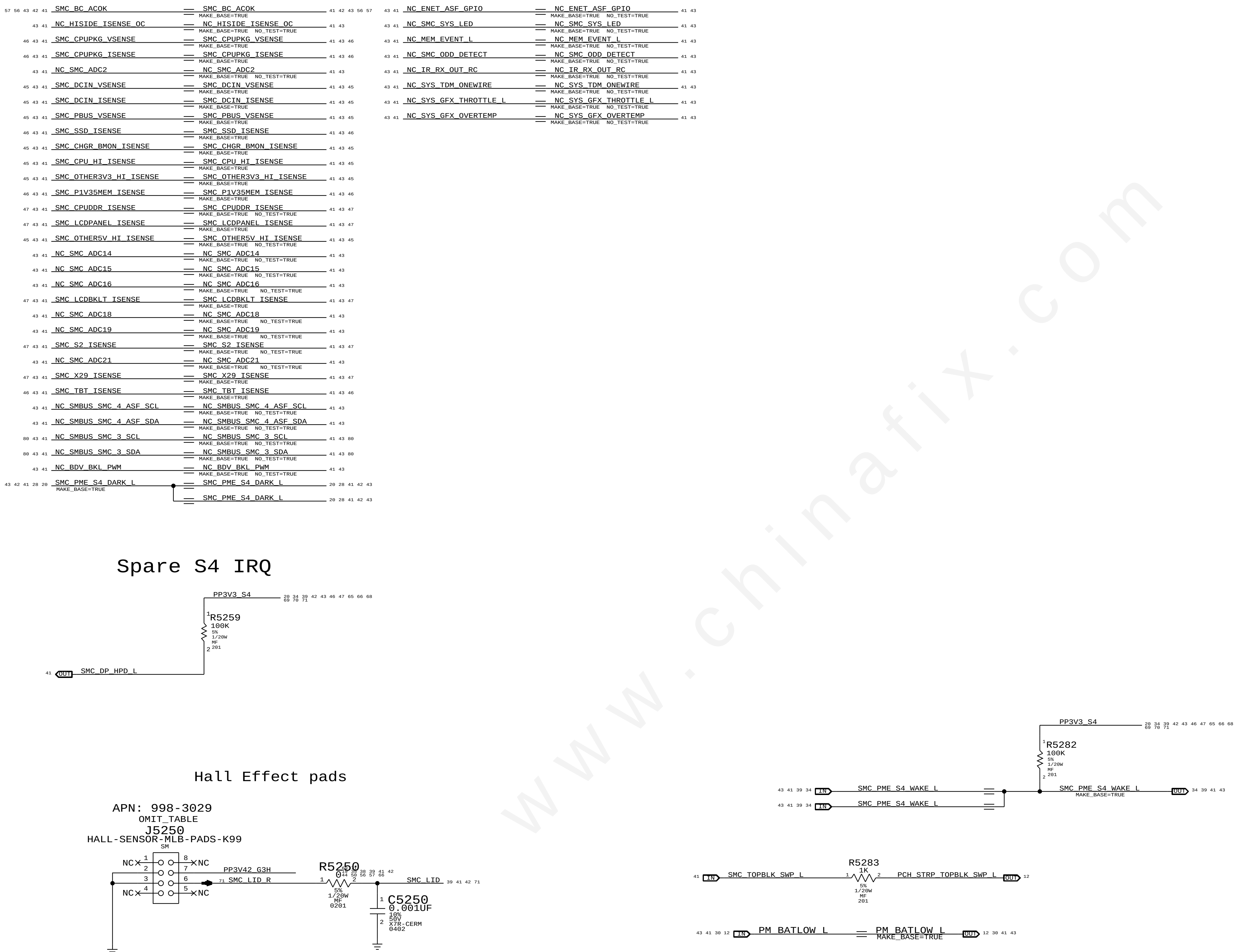
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SMC Reset "Button", Supervisor & AVREF Supply
R5127
PP3V42_G3H
PP3V42_G3H_SMC_SPVSR
C5127 4.7UF
NO STUFF
C5120 0.47UF
Mac Mini: 5V
Mobiles: 3.42V
U5110
VREF-3.3V-VDET-3.0V
SN0903049
CRITICAL
R5100 100K
SMC_TPAD_RST_L
SMC_ONOFF_L
SMC_MANUAL_RST_L
SMC_RESET_L
PP3V3_S5_AVREF_SMC
R5101
SILK_PART=SMC_RST
PLACE_SIDE=BOTTOM
C5101 0.01UF
C5125 10uF
C5126 0.01UF
GND_SMC_AVSS
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.
Debug Power "Buttons"
R5116
R5115
SILK_PART=PWR_BTN
SMC Crystal Circuit
R5110 2.49K
SMC_XTAL
SMC_XTAL_R
SMC_EXTAL
Y5110
12.000MHZ-30PPM-10PF-85C
C5110 12PF
C5111 12PF
SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ
PP1V05_S0
R5197 100K
SMC_VCCIO_CPU_DIV2
R5196 100K
SMC12 PECI SUPPORT
Q5130
DMN32D2LFB4
R5132
SMC_PECI_L
SMC_PECI_L_R
From SMC
R5133
R5131 330
R5134 43
CPU_PECI_R
CPU_PECI
To SMC
From/To CPU/PCH
CPU_PROCHOT_L
Q5159
DMN5L06VK-7
SMC_PROCHOT
PM_THRMTRIP_L_R
SMC_THRMTRIP
R5112 22
PM_CLK32K_SUSCLK_R
SMC_CLK32K
CPU_THRMTRIP_3V3
Q5158
MMBT3904LP-7
PM_THRMTRIP_B_L
R5158 3.3K
PM_THRMTRIP_L
PP3V42_G3H
PP3V3_S4
SMC_PME_S4_DARK_L R5169 100K
SMC_ONOFF_L R5170 10K
G3_POWERON_L R5172 10K
SMC_LID R5171 100K
SMC_TX_L R5173 10K
SMC_RX_L R5174 100K
SMC_DEBUGPRT_TX_L R5175 20K
SMC_DEBUGPRT_RX_L R5176 20K
SMC_TMS R5177 10K
SMC_TDO R5178 10K
SMC_TDI R5179 10K
SMC_TCK R5180 10K
SMC_BIL_BUTTON_L R5181 10K
SMC_BC_ACOK R5187 470K
SMC_S5_PWRGD_VIN R5192 100K
SMS_INT_L R5193 10K
CPU_THRMTRIP_3V3 R5194 100K
SPI_DESCRIPTOR_OVERRIDE_L R5195 10K
SMC_ROMBOOT
R5188 1K
SMC_THRMTRIP R5186 10K
SMC_DELAYED_PWRGD R5191 100K
SMC_PM_G2_EN R5198 100K
SMC_ADAPTER_EN R5185 10K
SMC_S4_WAKESRC_EN R5190 100K
PP3V3_WLAN
WIFI_EVENT_L R5189 10K
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SYNC_DATE=11/12/2012
SMC Shared Support
Apple Inc.
<SCH_NUM>
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	

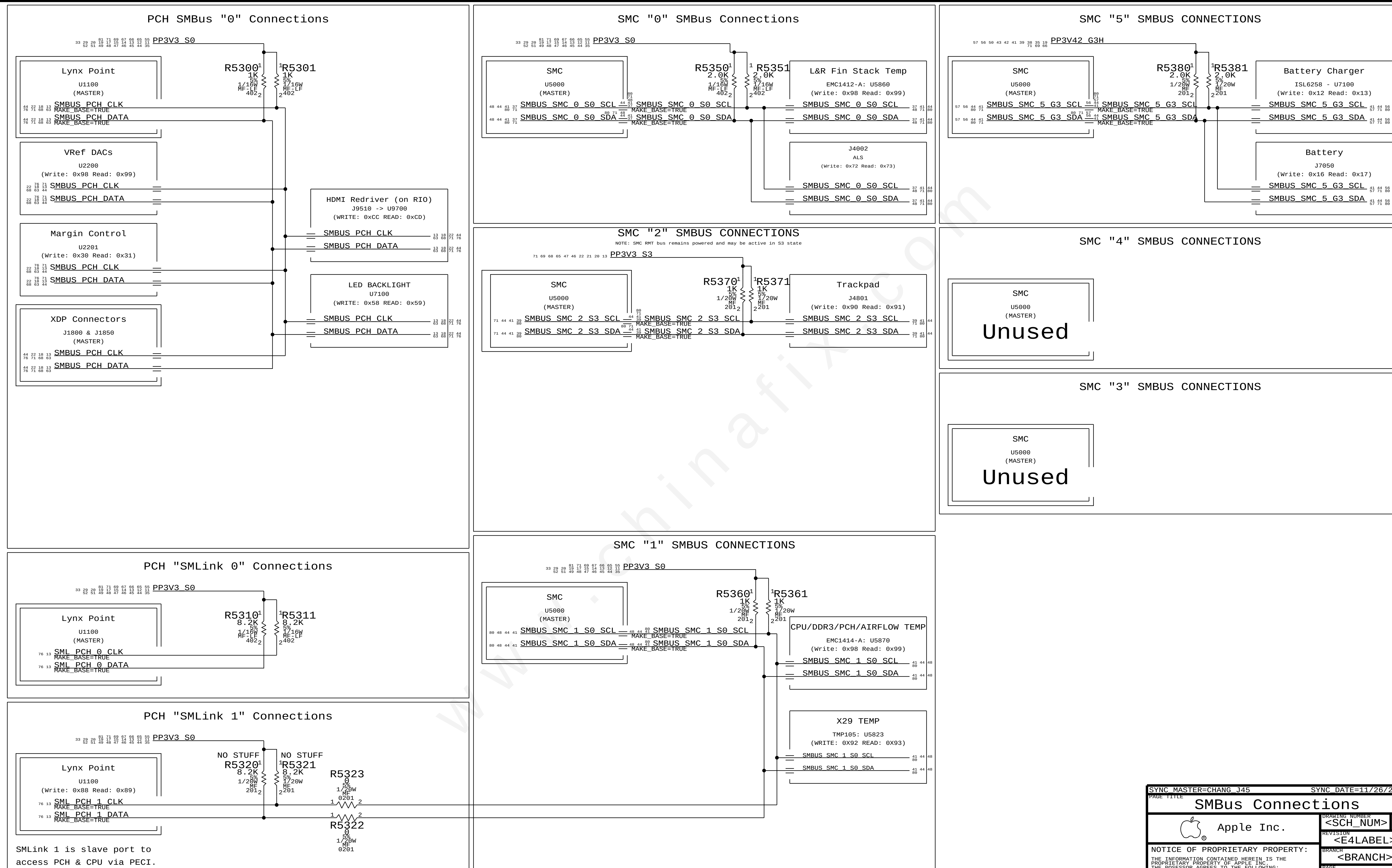
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SMC Project Support

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SMBus Connections

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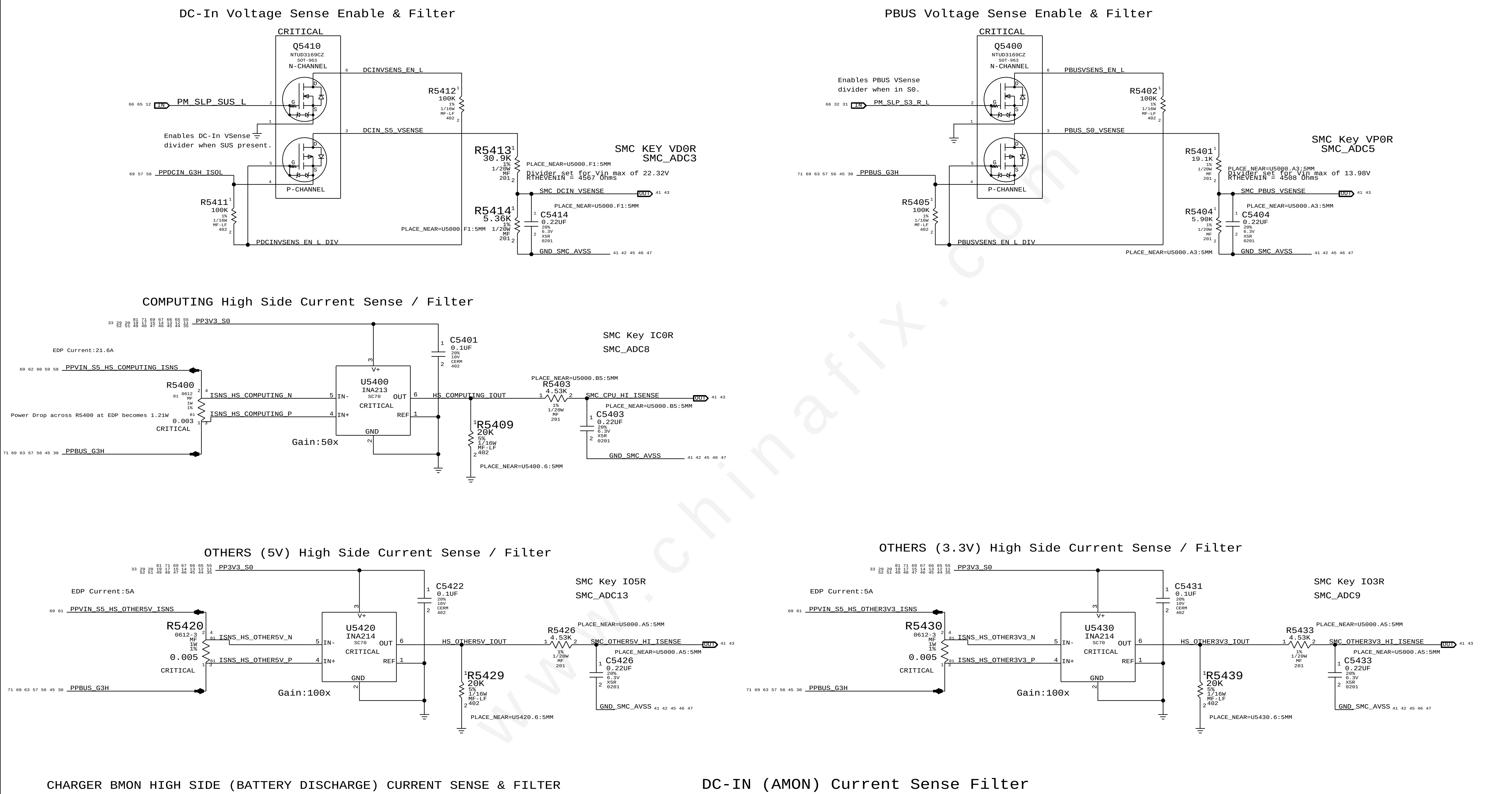
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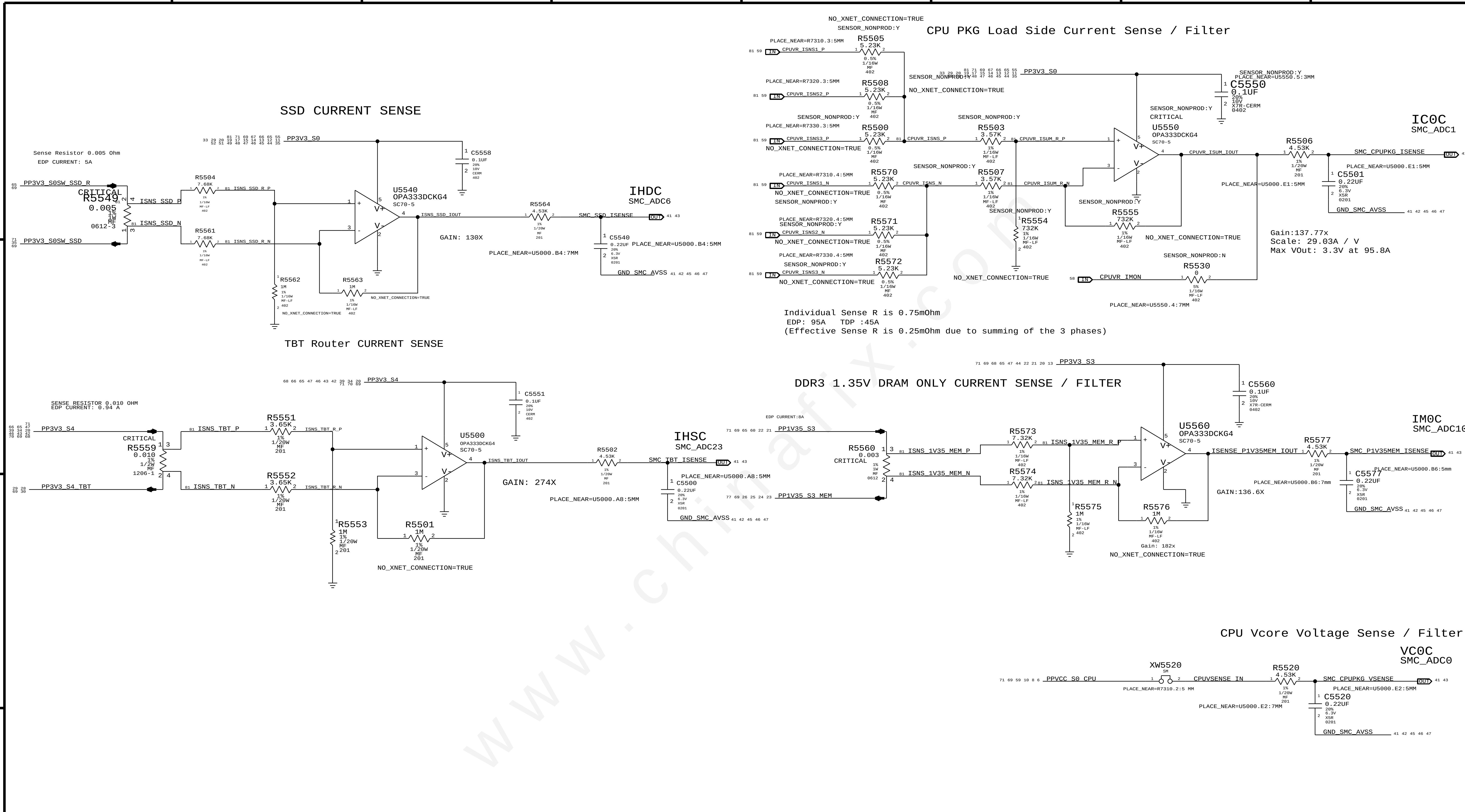
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Load Side Voltage and Current Sensing

Apple Inc.

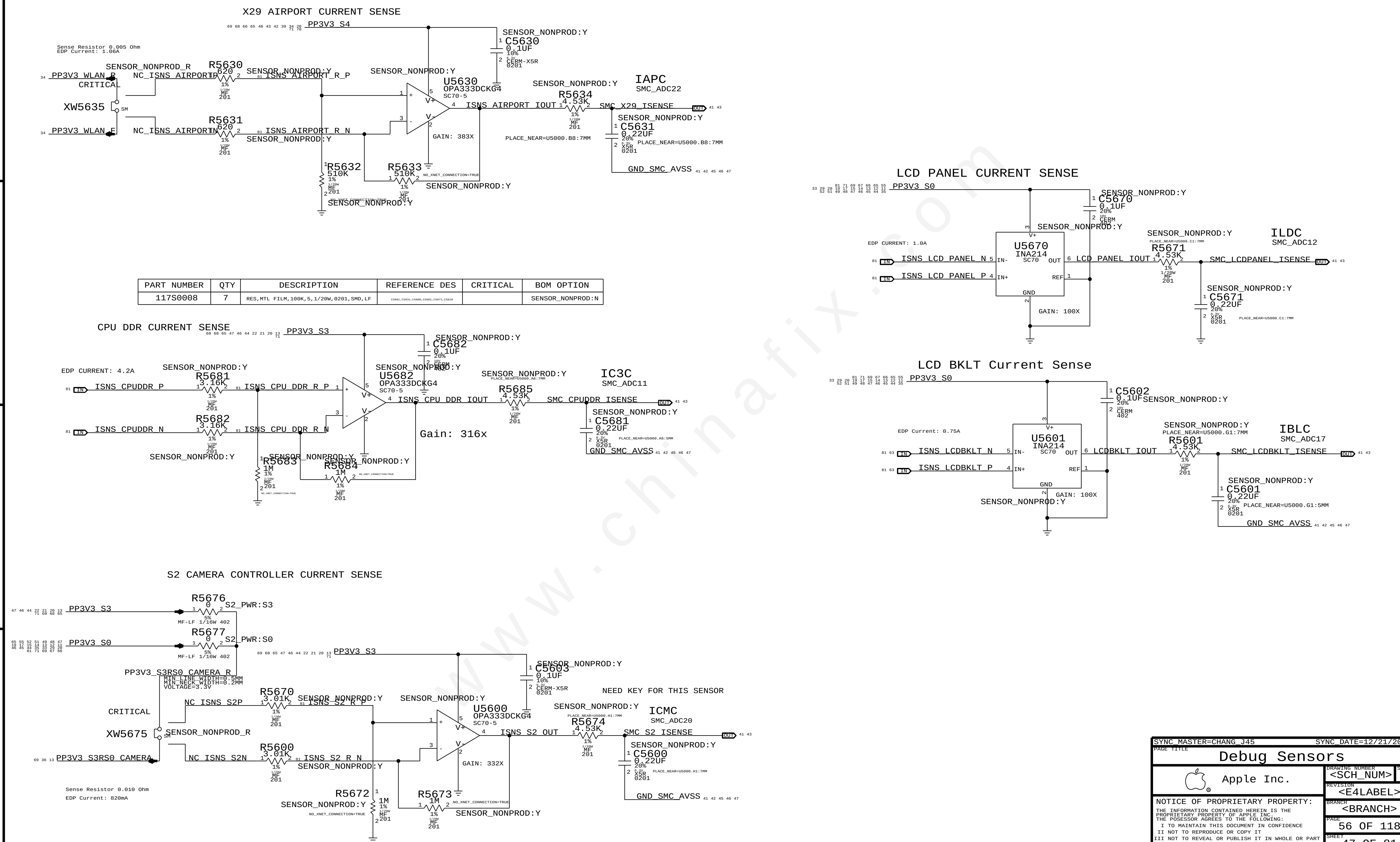
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	7	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF	C5601,C5631,C5600,C5681,C5671,C5618		SENSOR_NONPROD:N

SYNC_MASTER=CHANG_J45 SYNC_DATE=12/21/2012

PAGE TITLE
Debug Sensors

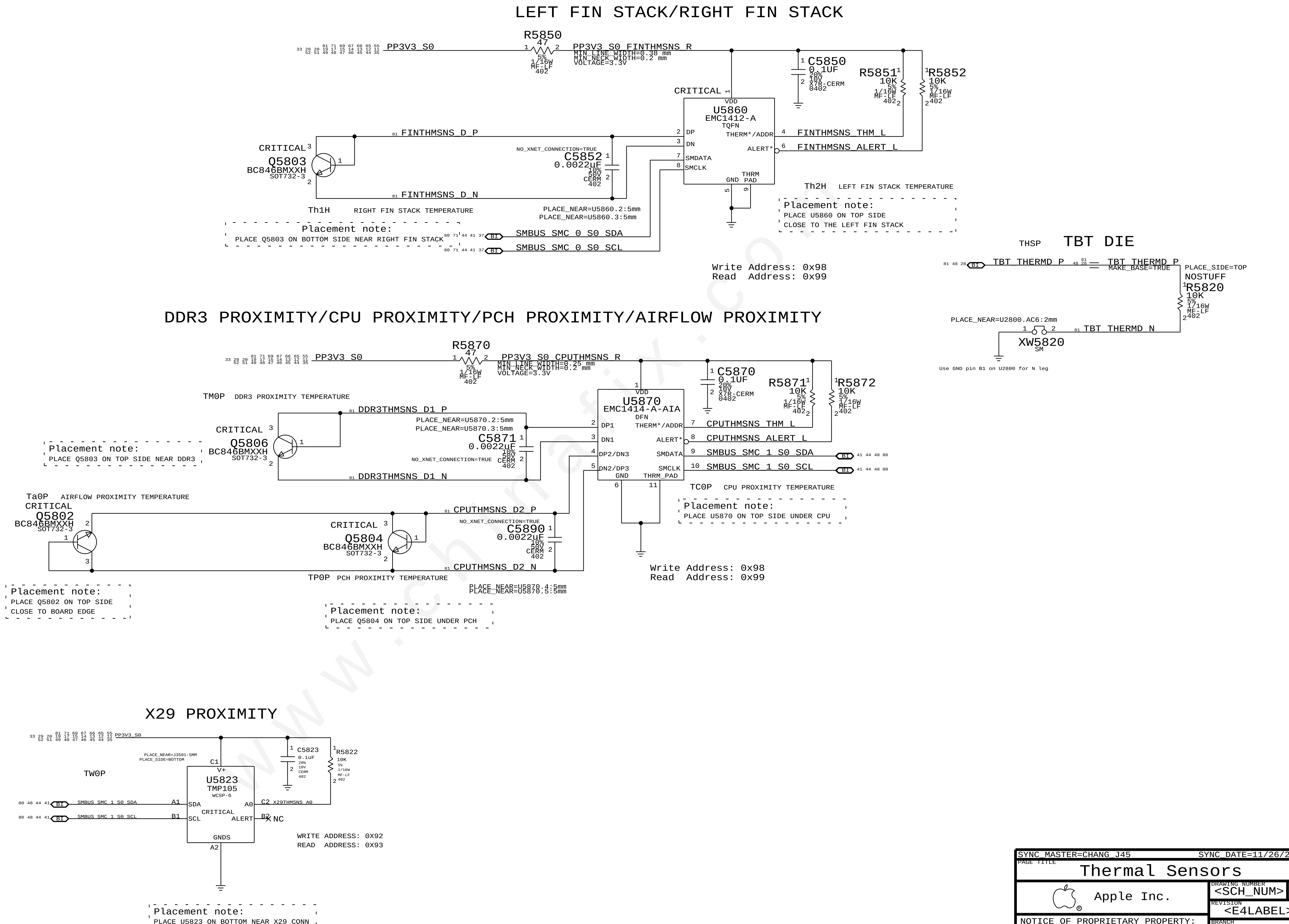
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LEFT FIN STACK/RIGHT FIN STACK



SYNC_MASTER=CHANG_J45 SYNC_DATE=11/26/2012

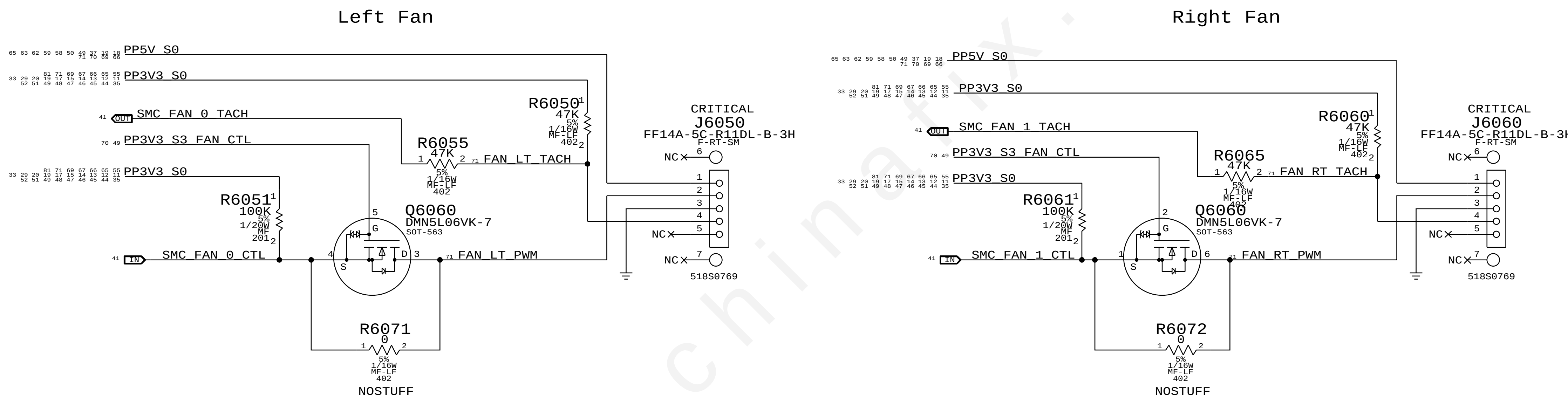
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Thermal Sensors

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Fan Connectors

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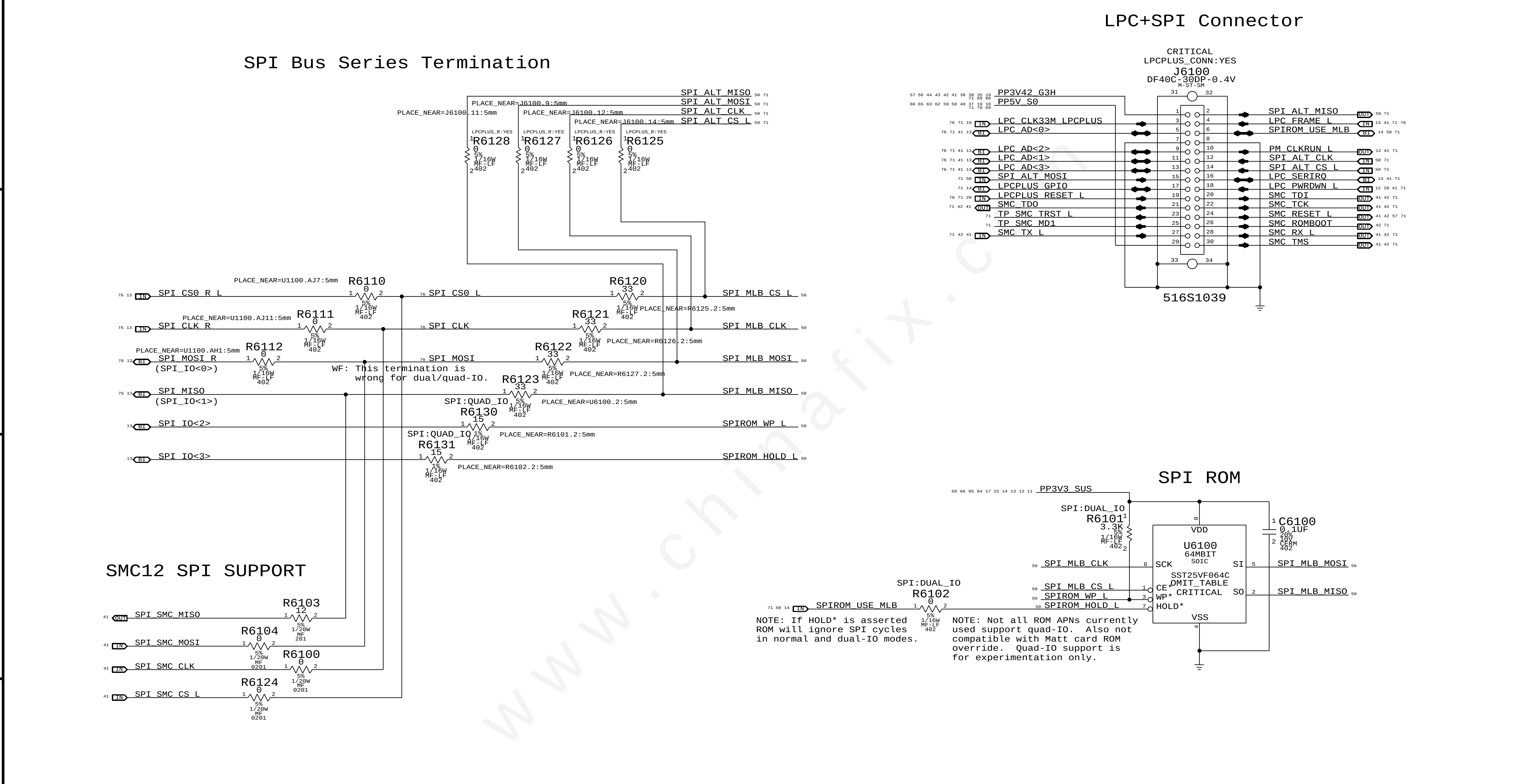
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SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: SPI ROM / LPC+SPI Conn.

Apple Inc.

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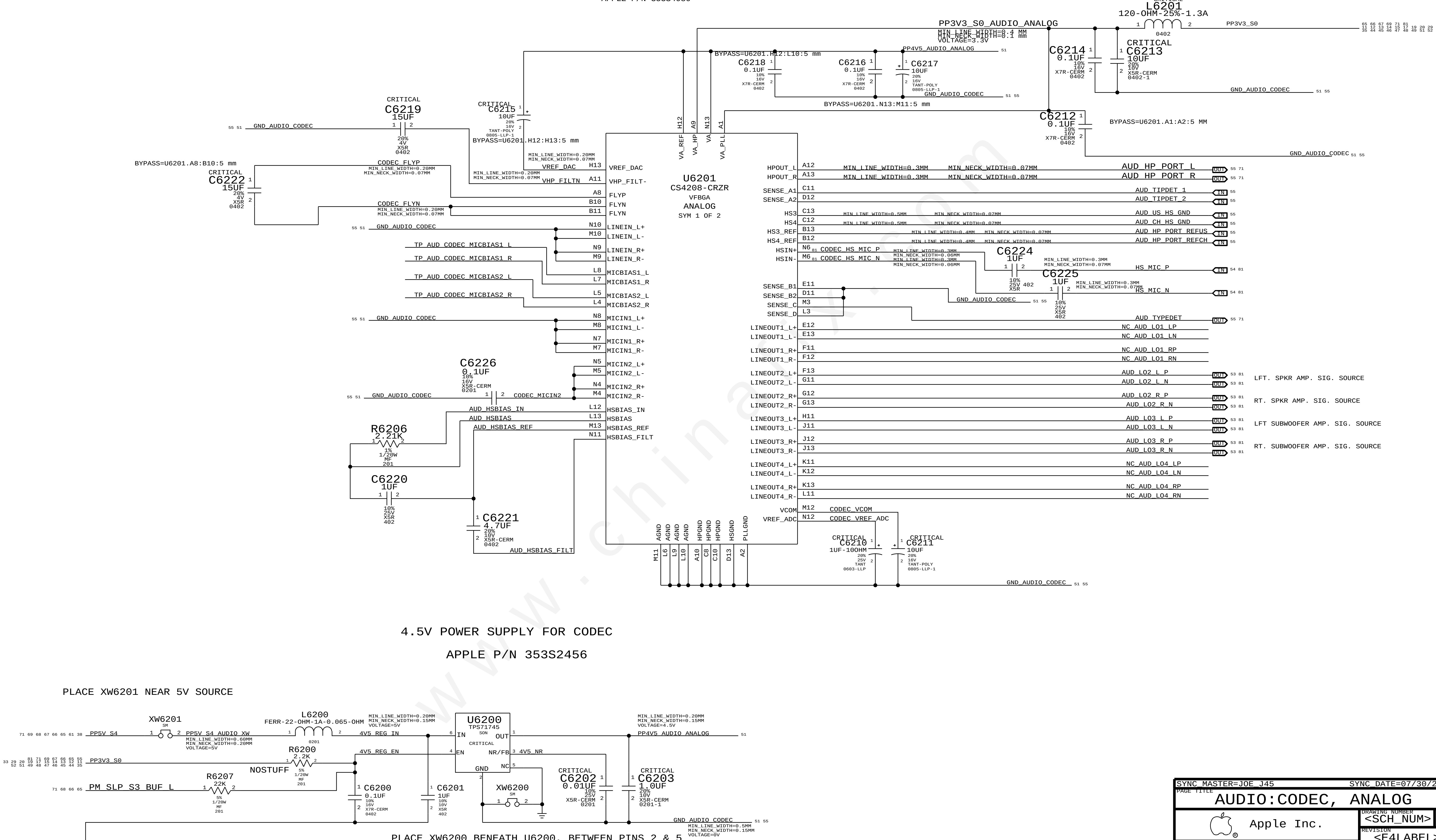
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AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE

AUDIO:CODEC, ANALOG

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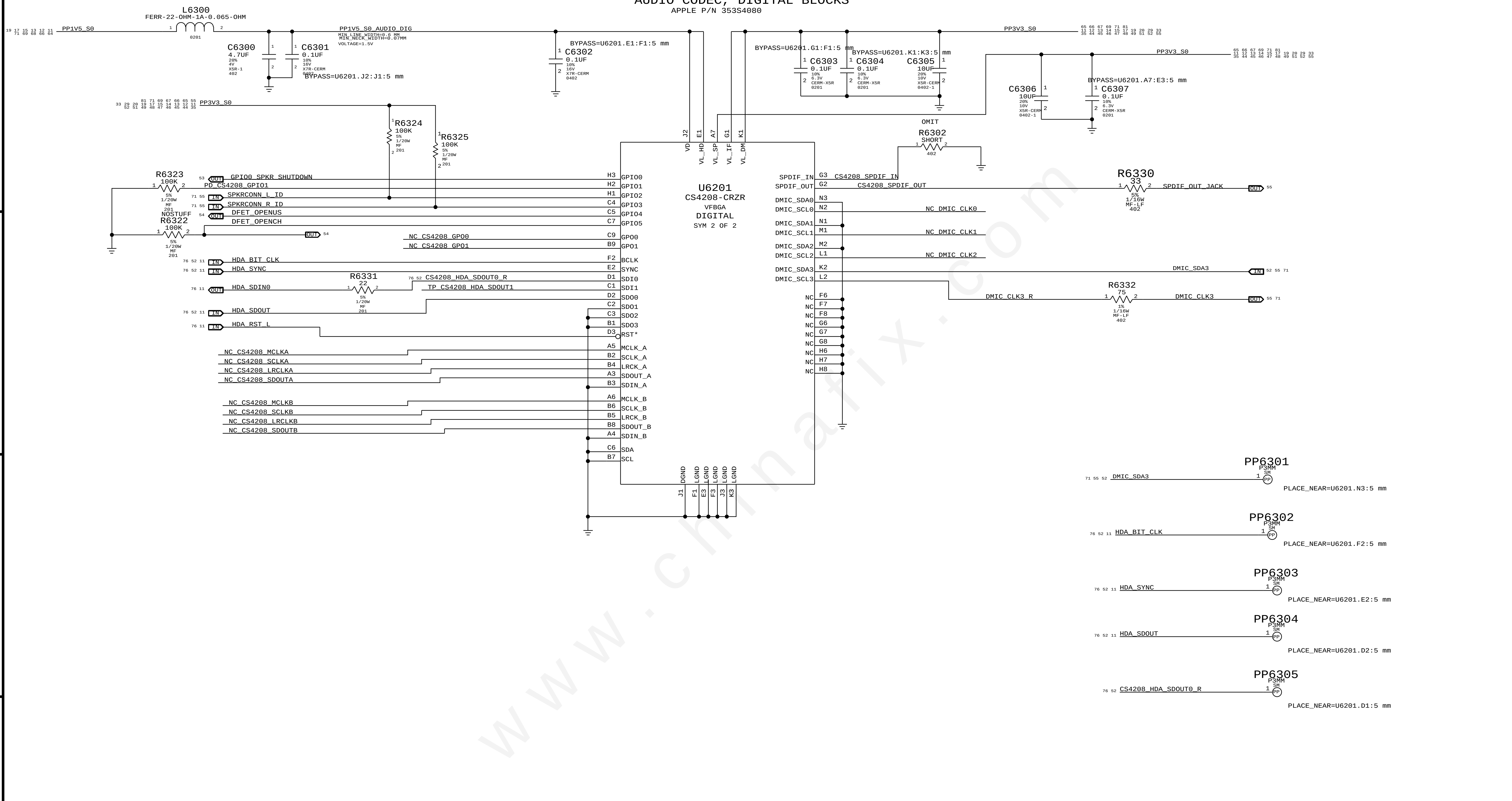
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AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE

AUDIO:CODEC, DIGITAL

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DRAWING NUMBER <SCH_NUM> SIZE D

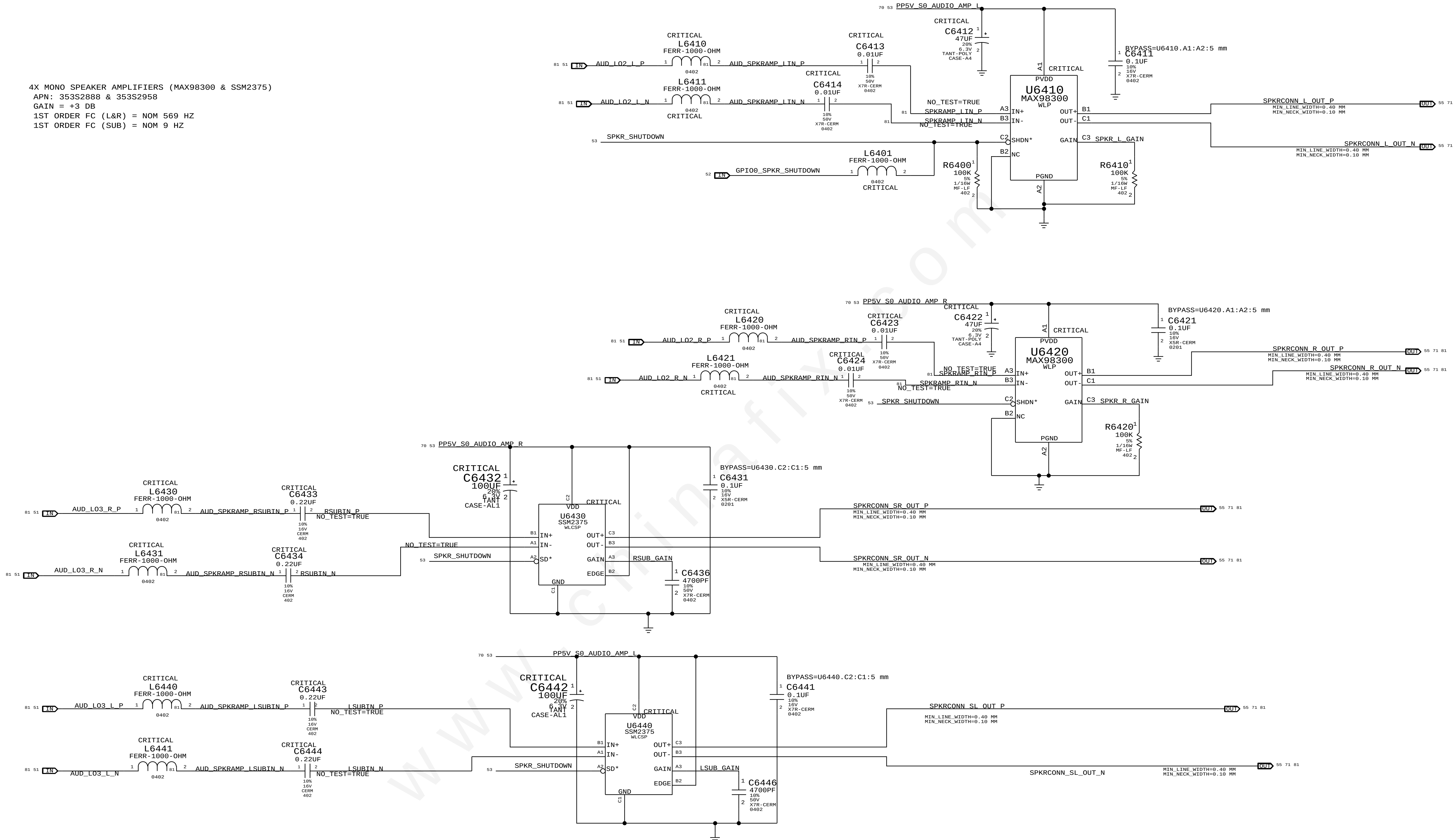
REVISION <E4LABEL>

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4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

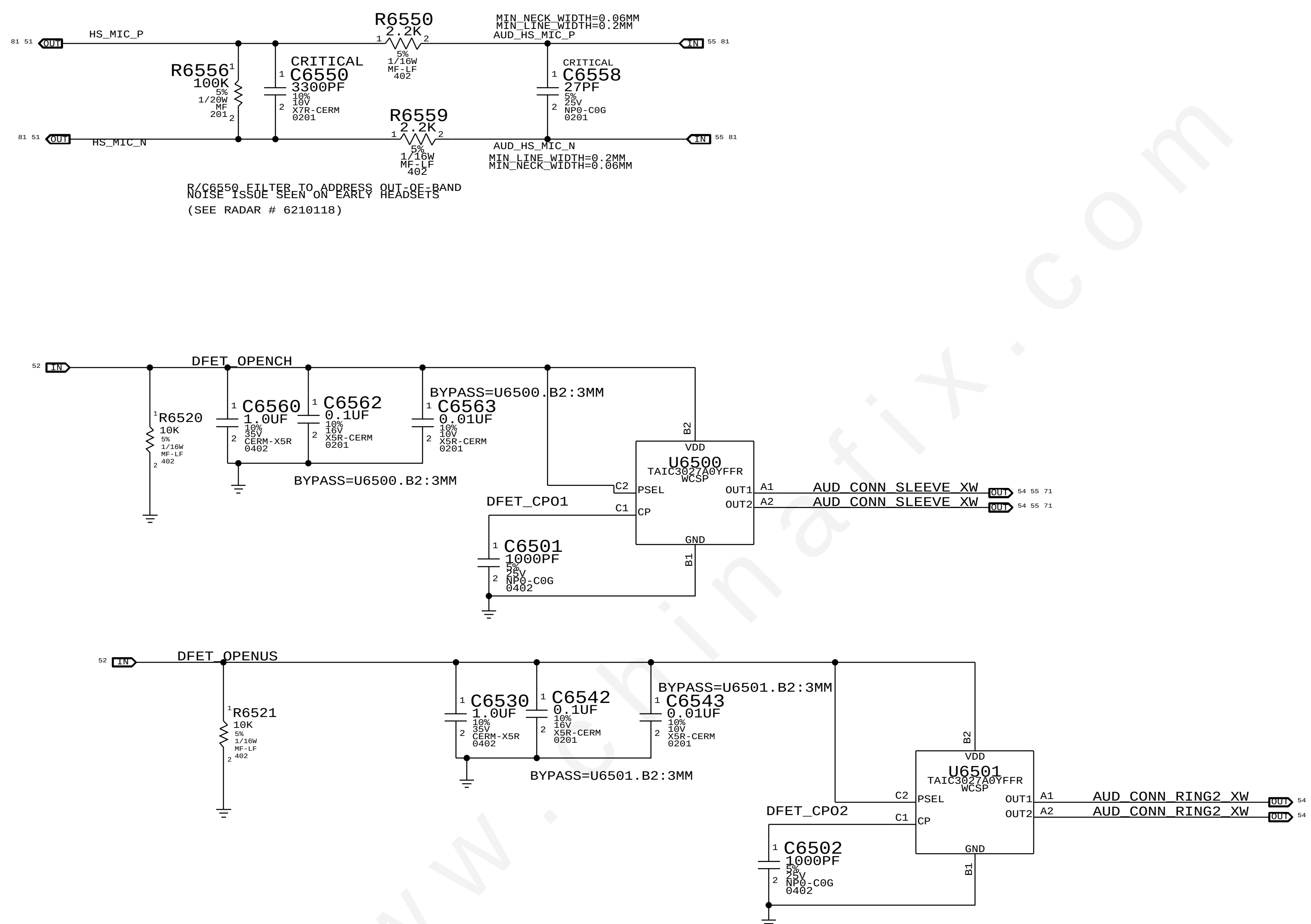
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AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE

AUDIO: JACK

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CODEC OUTPUT SIGNAL PATHS

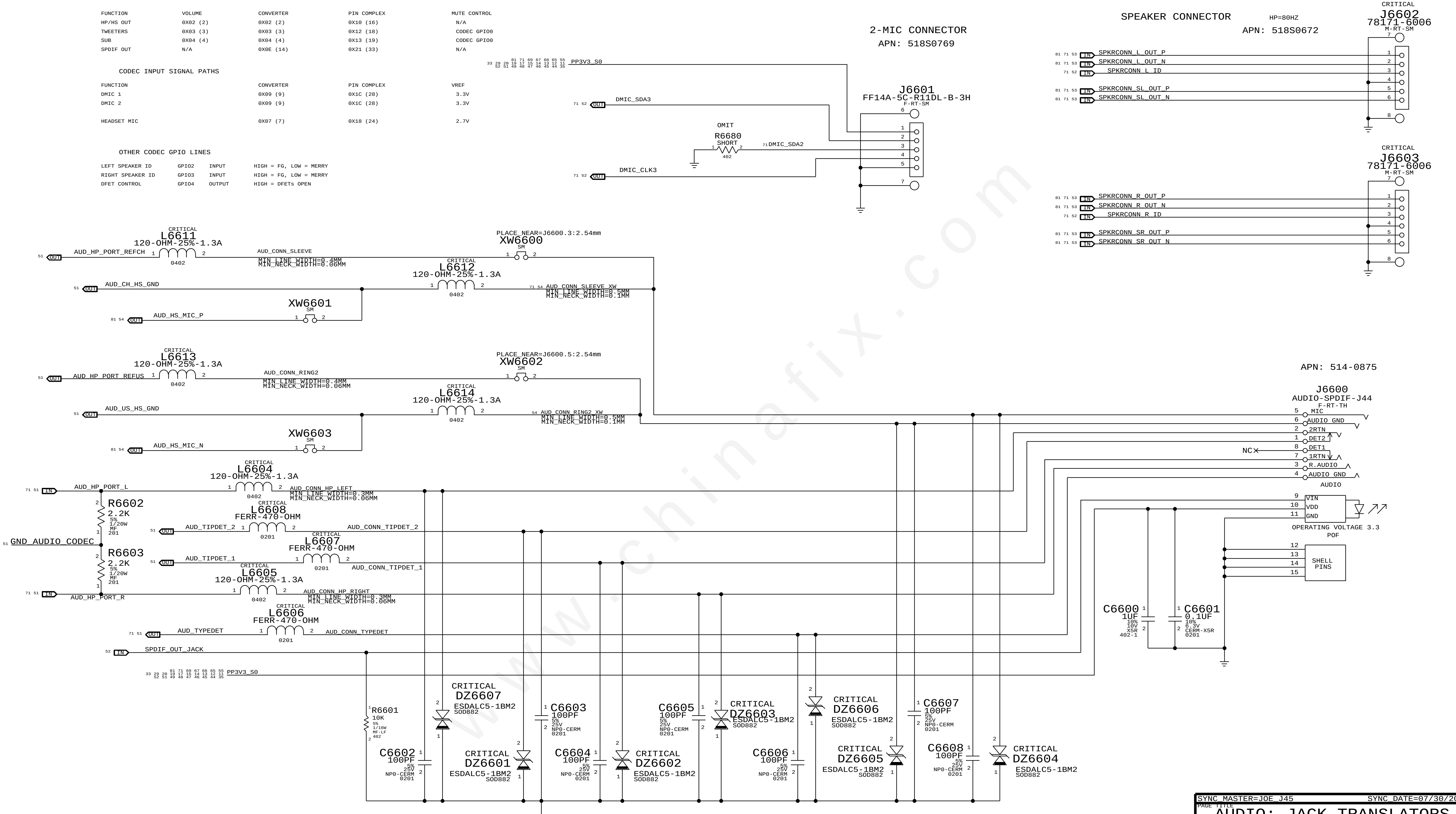
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

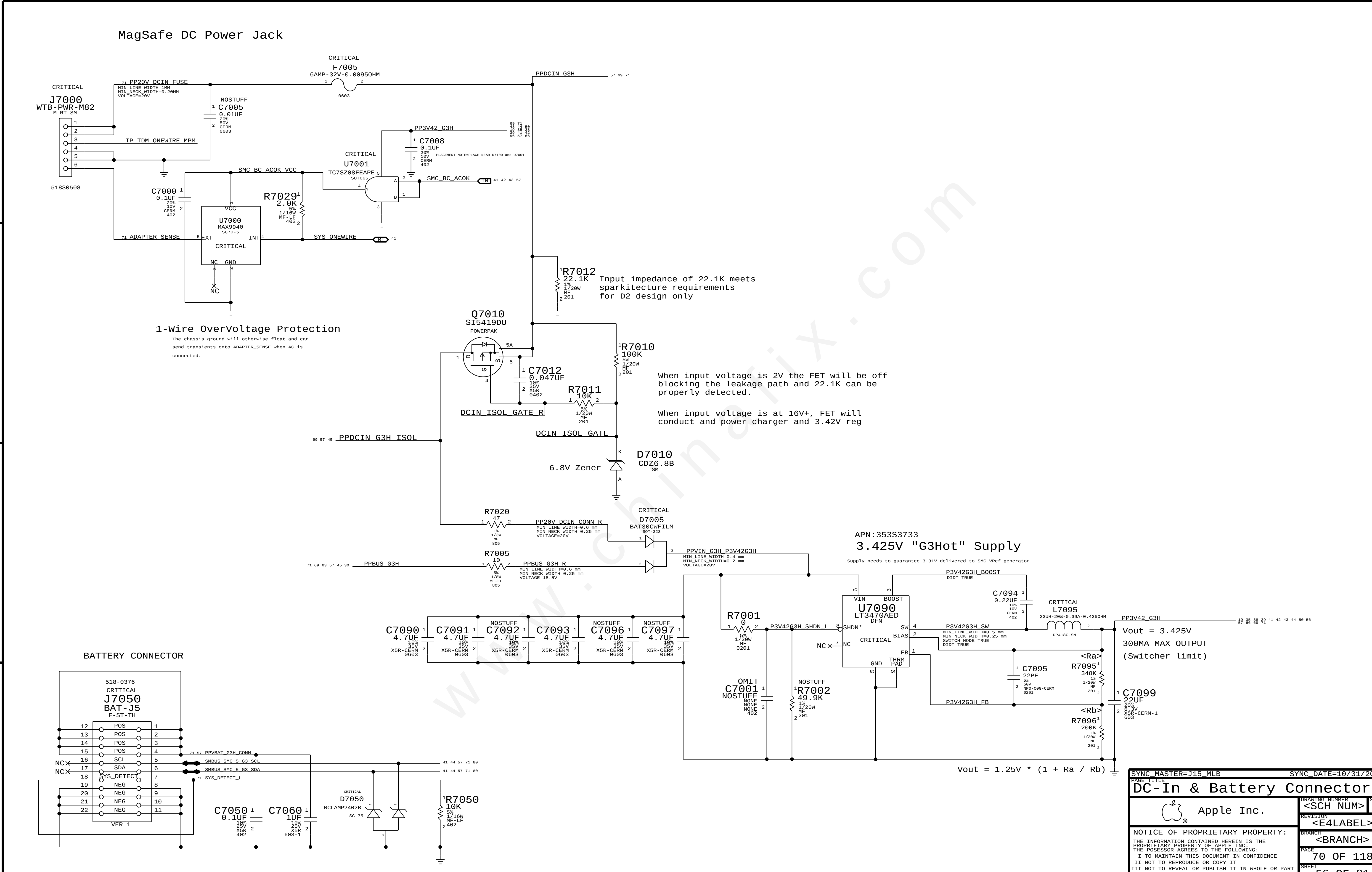
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AUDIO: JACK TRANSLATORS

Apple Inc.

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SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

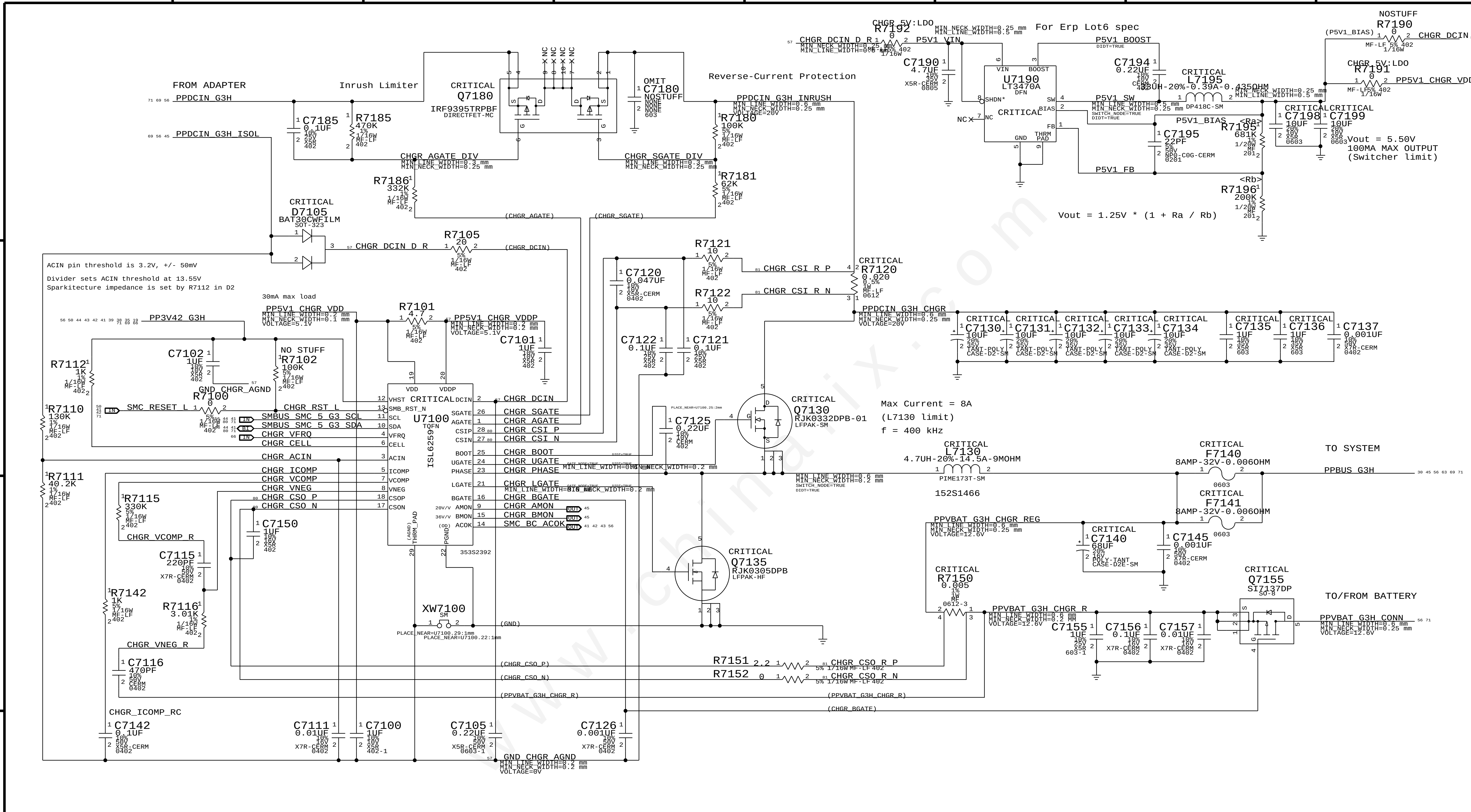
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SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
PBus Supply & Battery Charger

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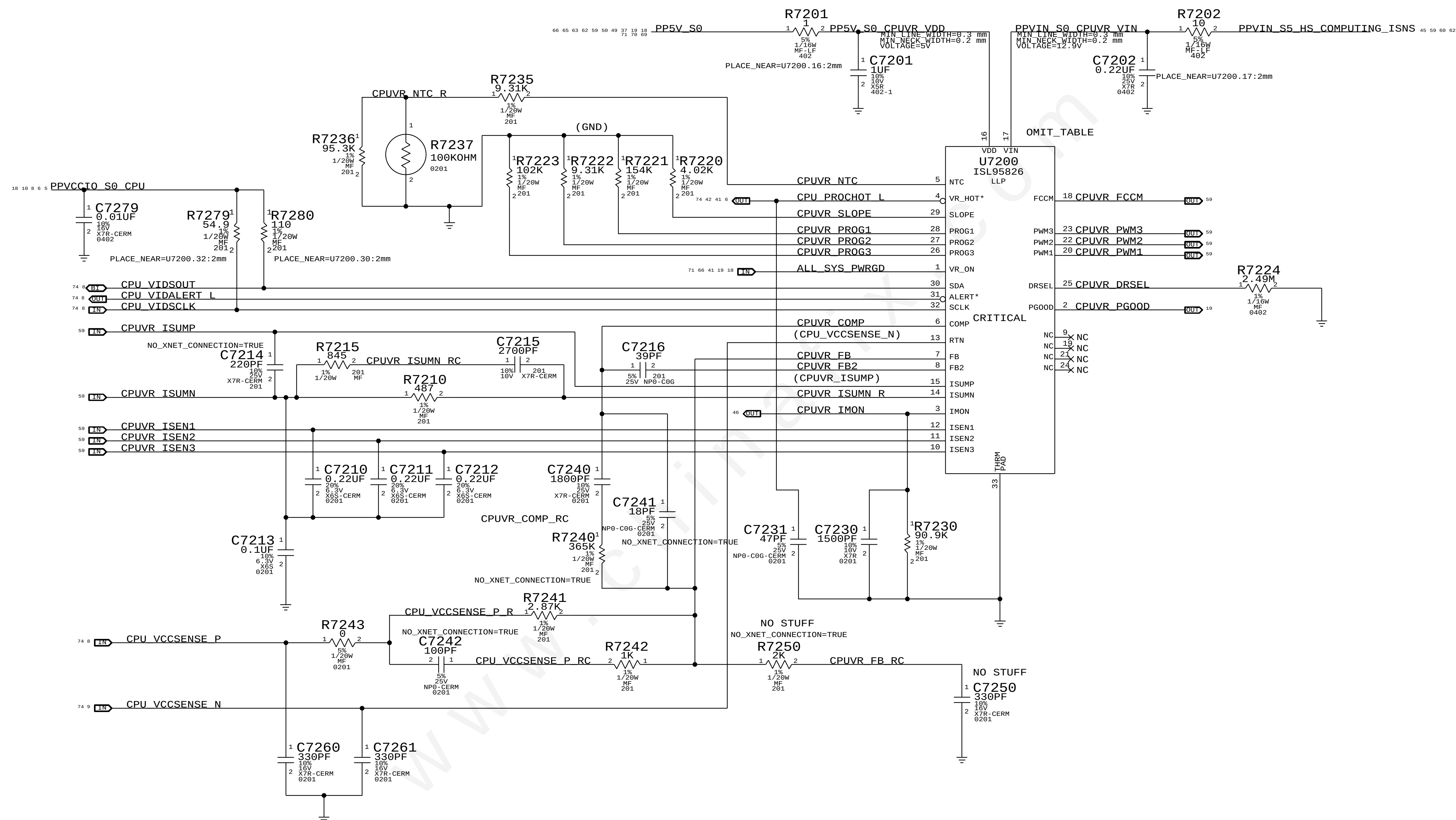
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC,ISL95826R6200,PWM,PGOOD,SCREEN,32P,QFN	U7200	CRITICAL	



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

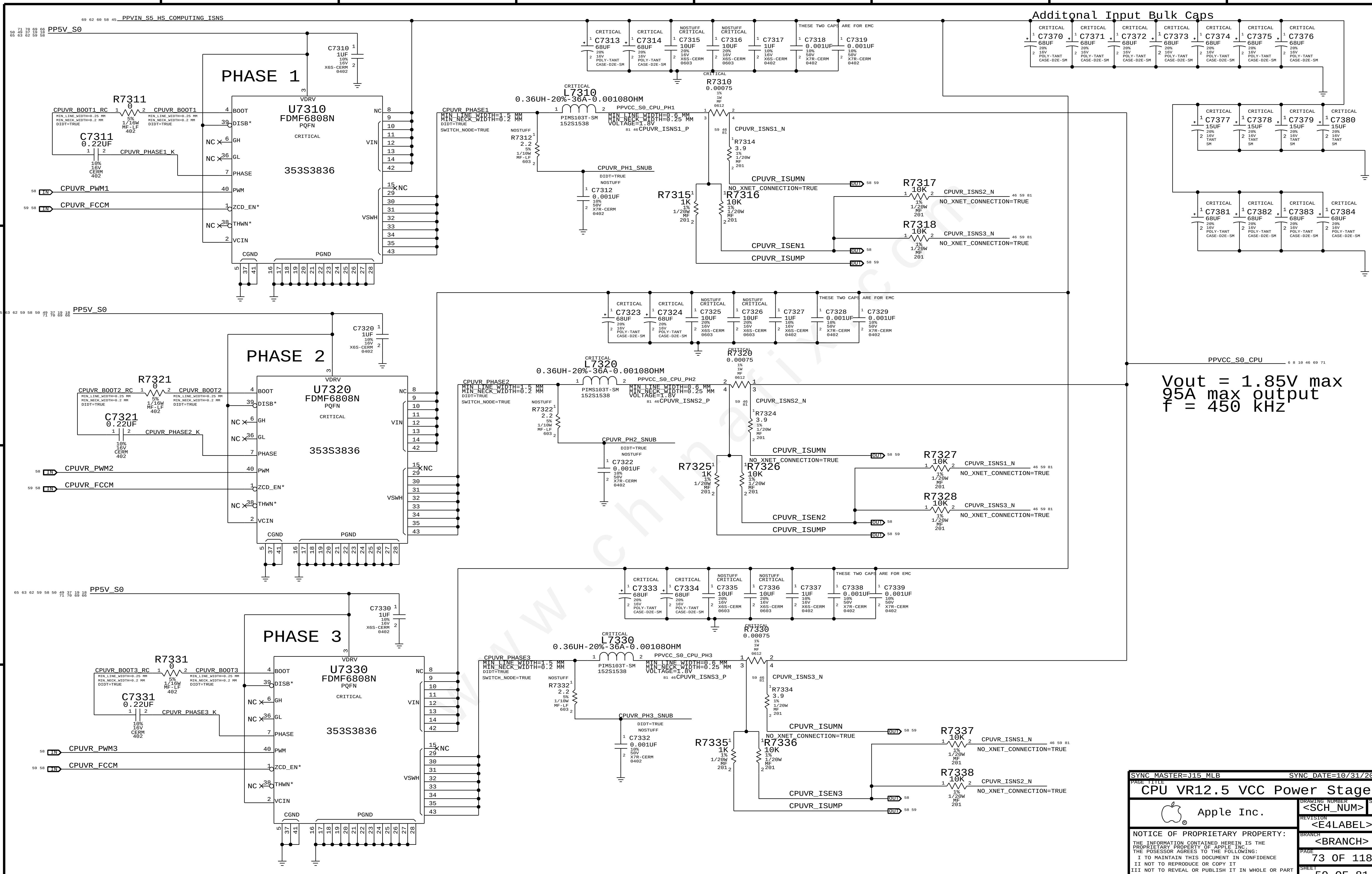
CPU VR12.5 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

CPU VR12.5 VCC Power Stage

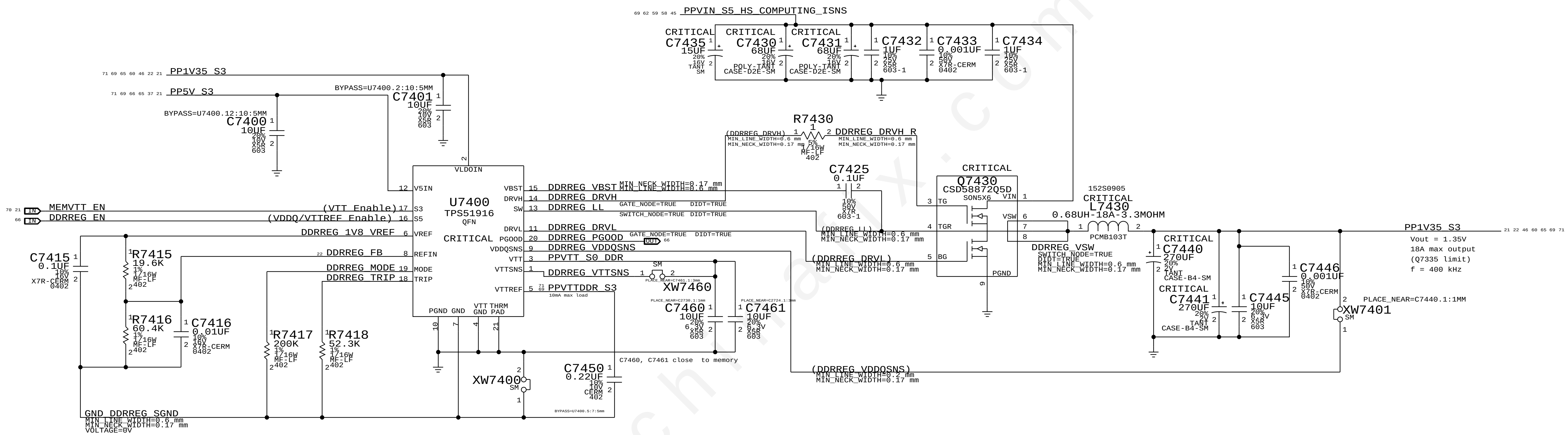
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DDR3L (1V35 S3) REGULATOR



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PAGE TITLE

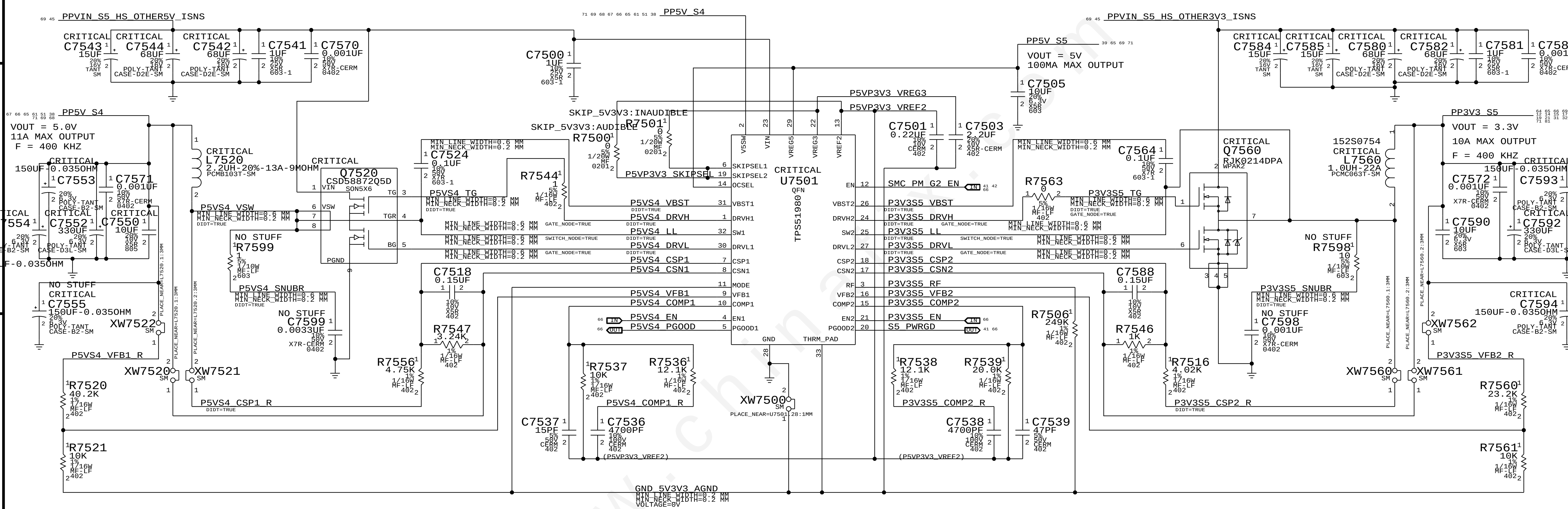
1.35V DDR3L SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

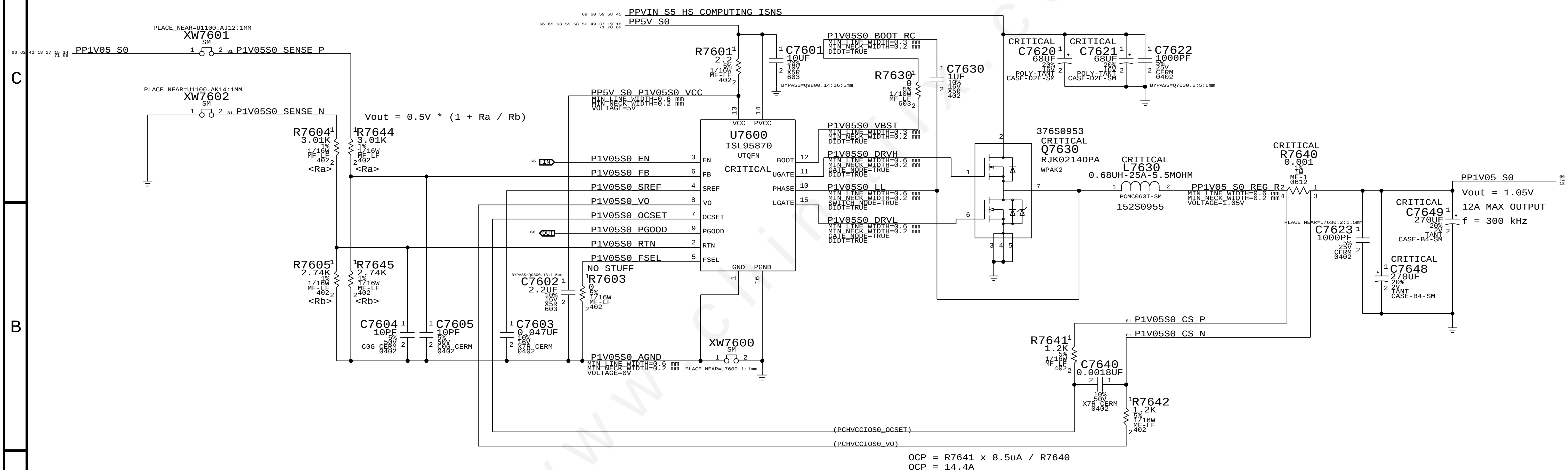
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SYNC_MASTER=J15_MLB	SYNC_DATE=10/31/2012
PAGE TITLE	
5V / 3.3V Power Supply	
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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1V05 S0 REGULATOR



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

1V05V POWER SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

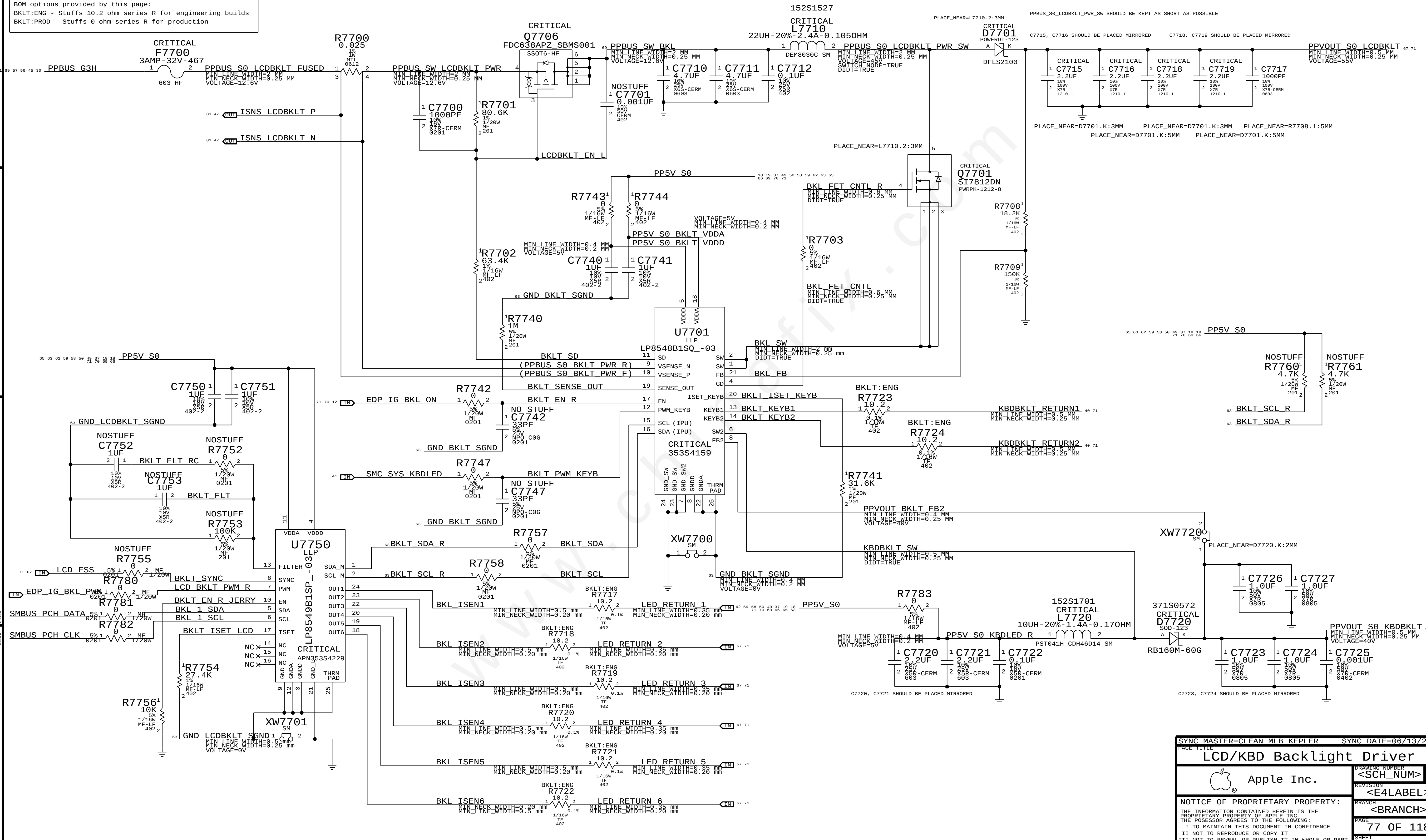
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Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	8	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7717,R7718,R7719,R7720,R7721,R7722,R7723,R7724		BKLT:PROD



SYNC_MASTER=CLEAN_MLB_KEPLER SYNC_DATE=06/13/2013

PAGE TITLE
LCD/KBD Backlight Driver

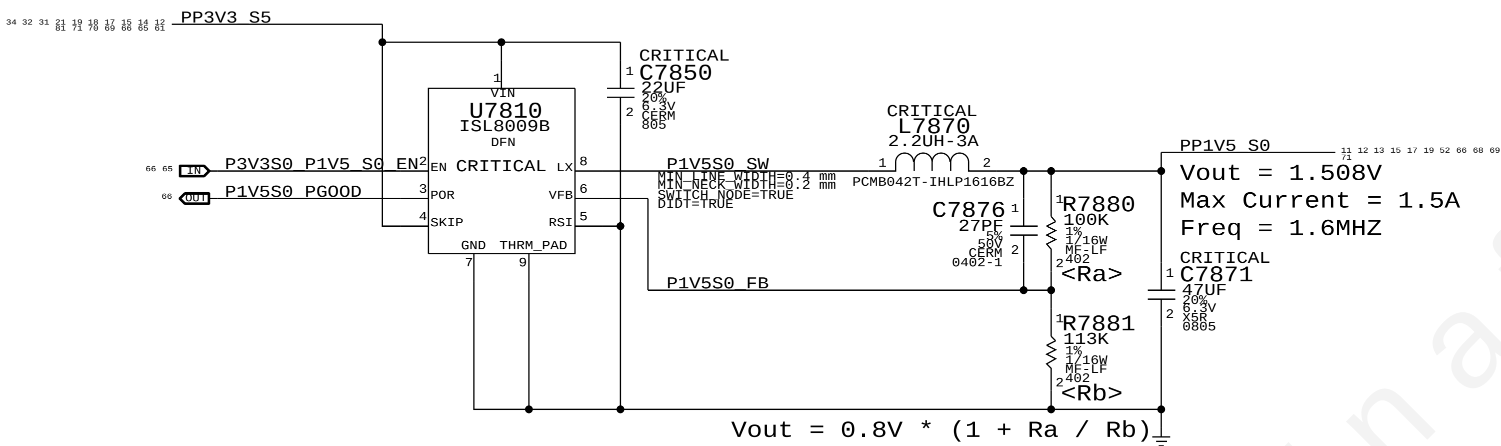
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1.5V S0 Regulator

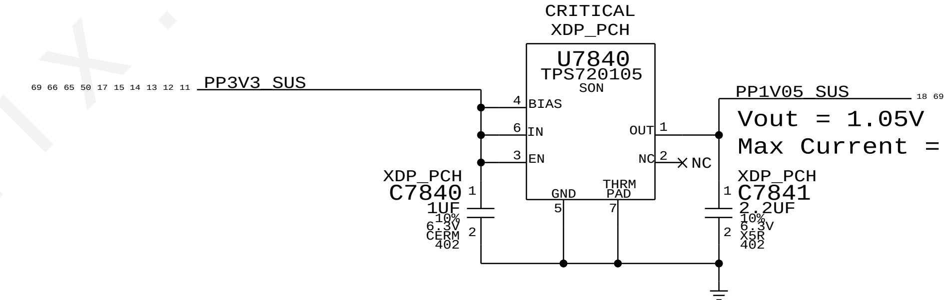


Vout = 1.508V
Max Current = 1.5A
Freq = 1.6MHZ

Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



Vout = 1.05V
Max Current = 0.35A

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
Misc Power Supplies

Apple Inc.

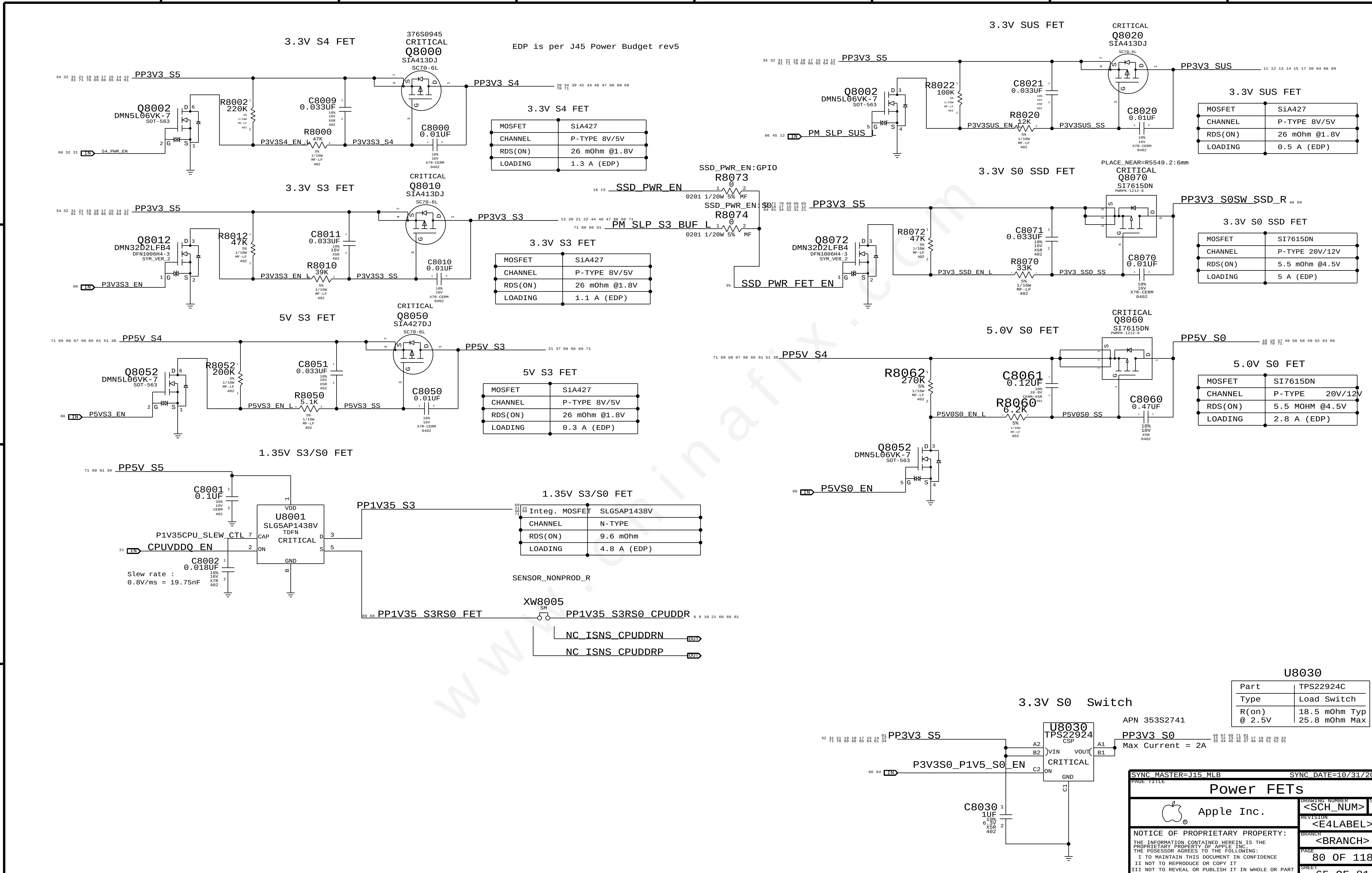
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3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

5V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

3.3V S0 SSD FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

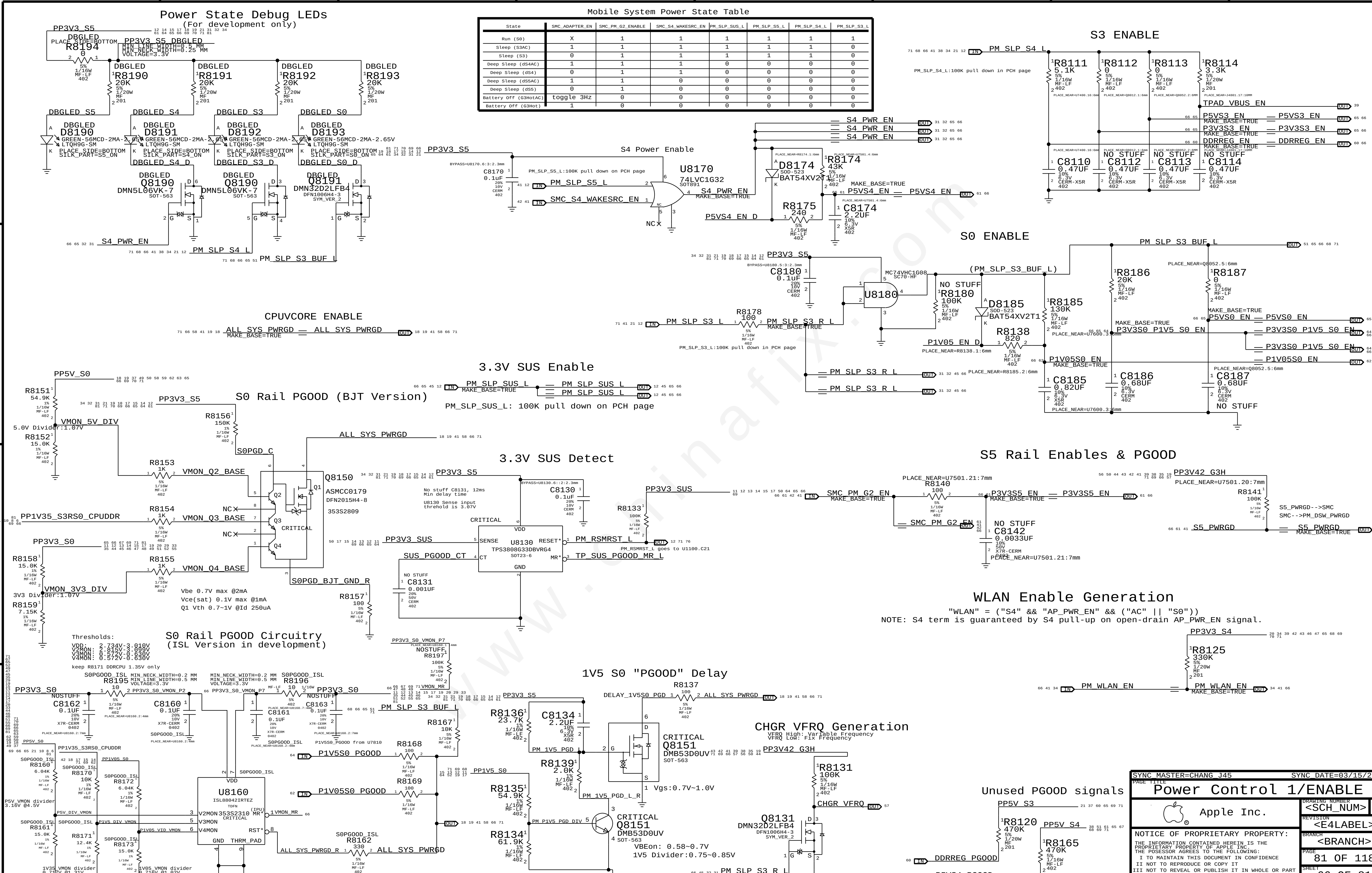
Power FETs

DRAWING NUMBER <SCH_NUM> SIZE D

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Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

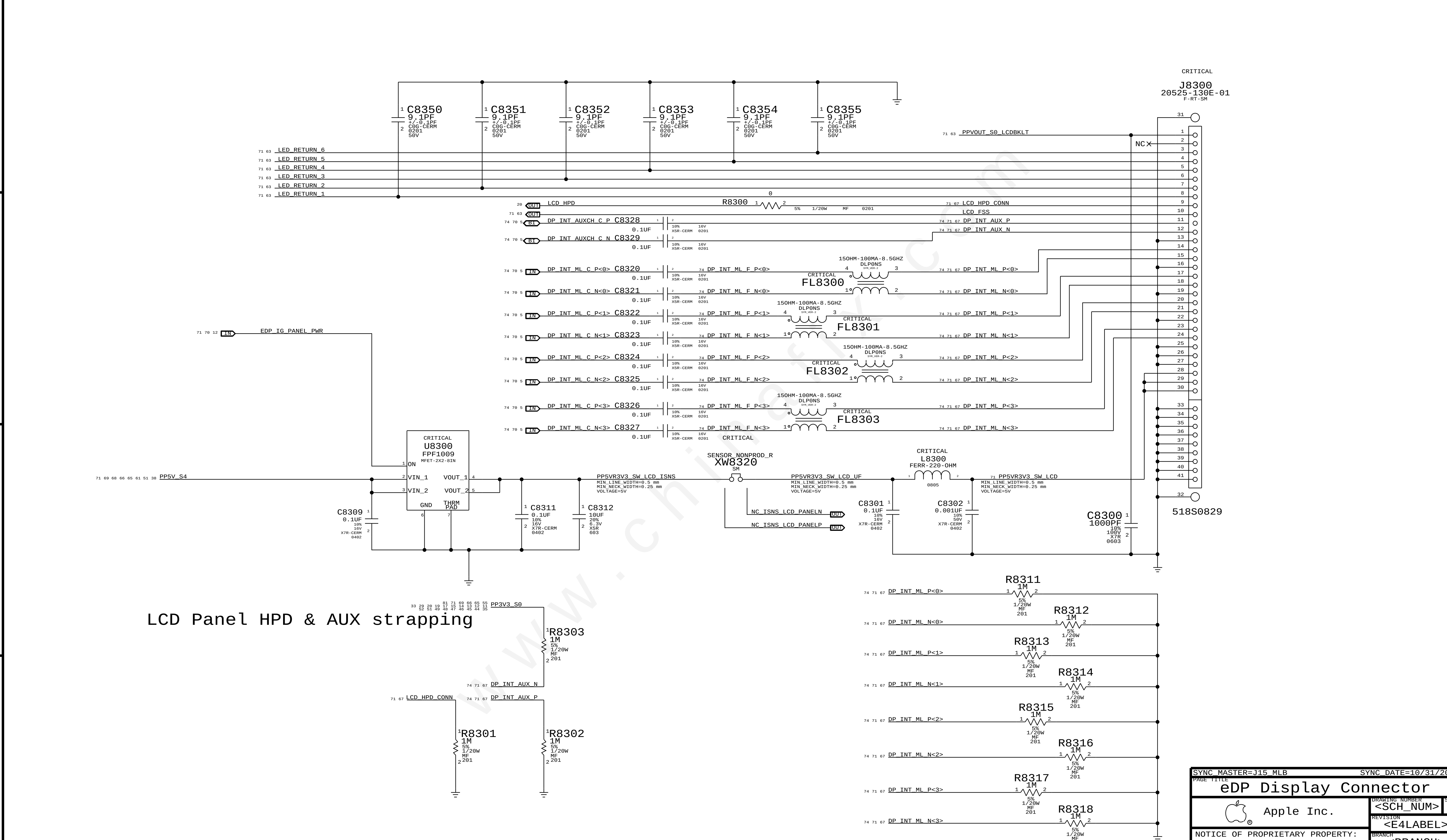
SYNC_MASTER=CHANG_J45 SYNC_DATE=03/15/2013

PAGE TITLE
Power Control 1/ENABLE

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LCD PANEL INTERFACE (eDP)



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

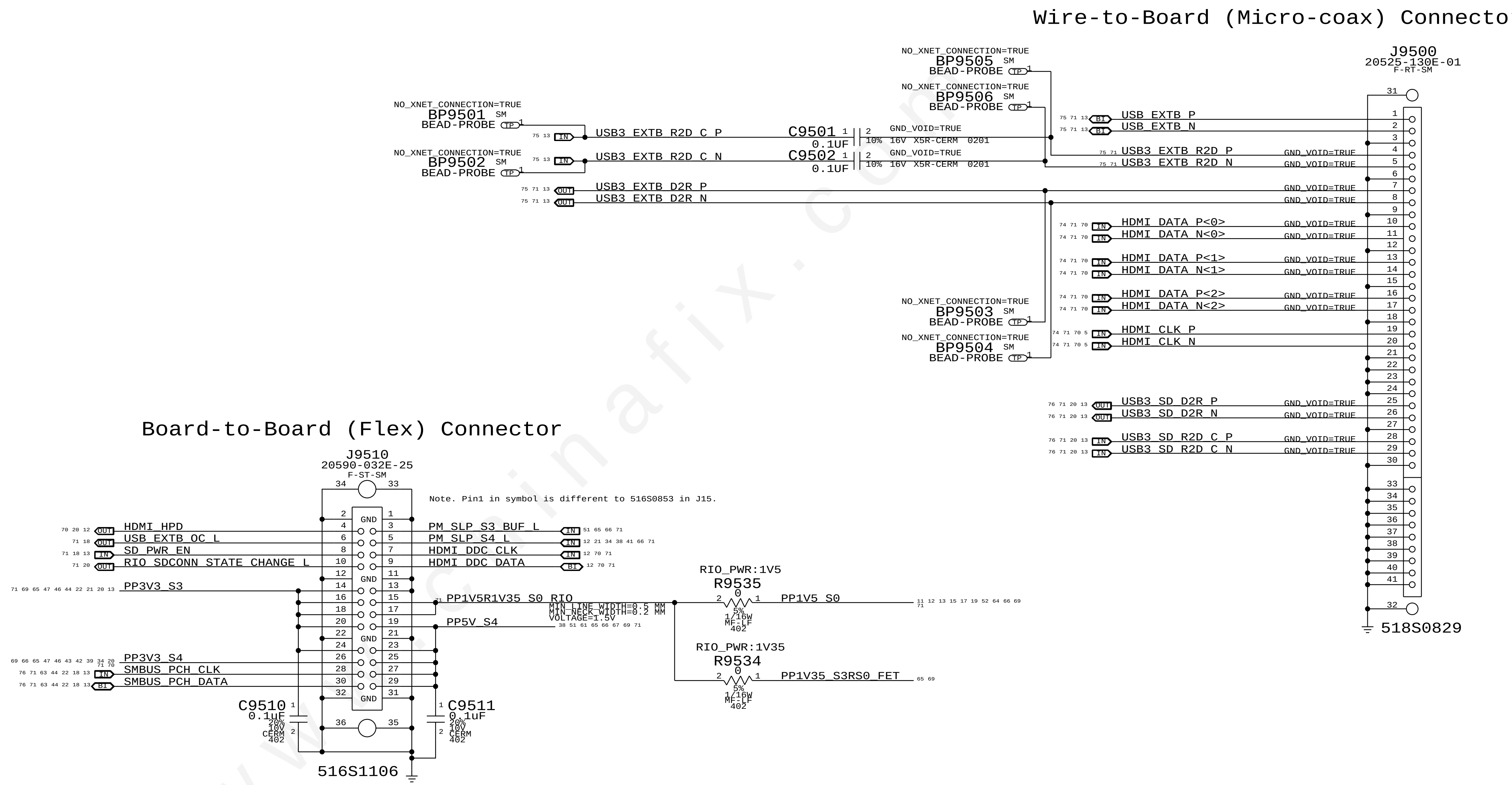
PAGE TITLE: eDP Display Connector

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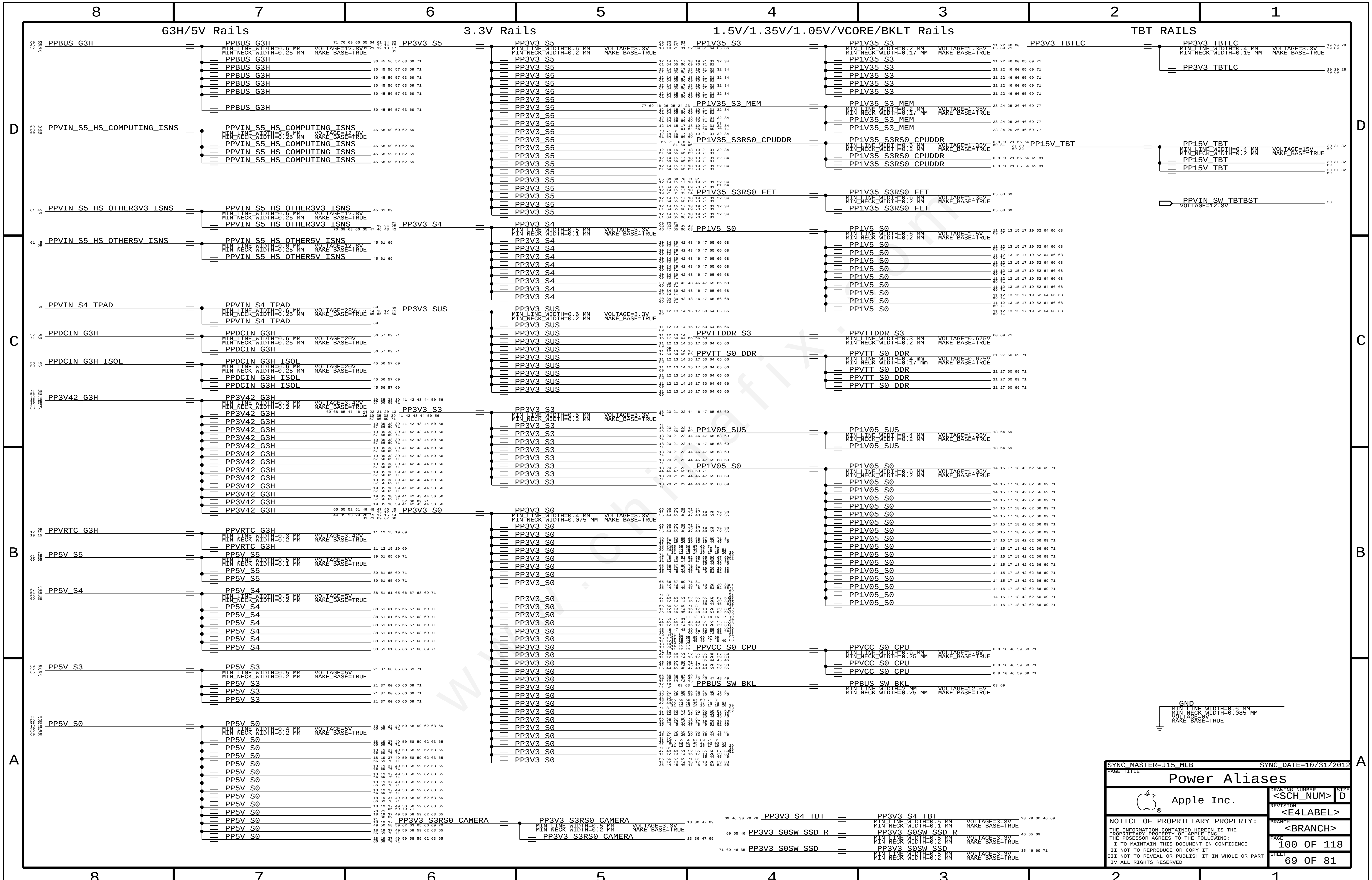
RIO Connectors

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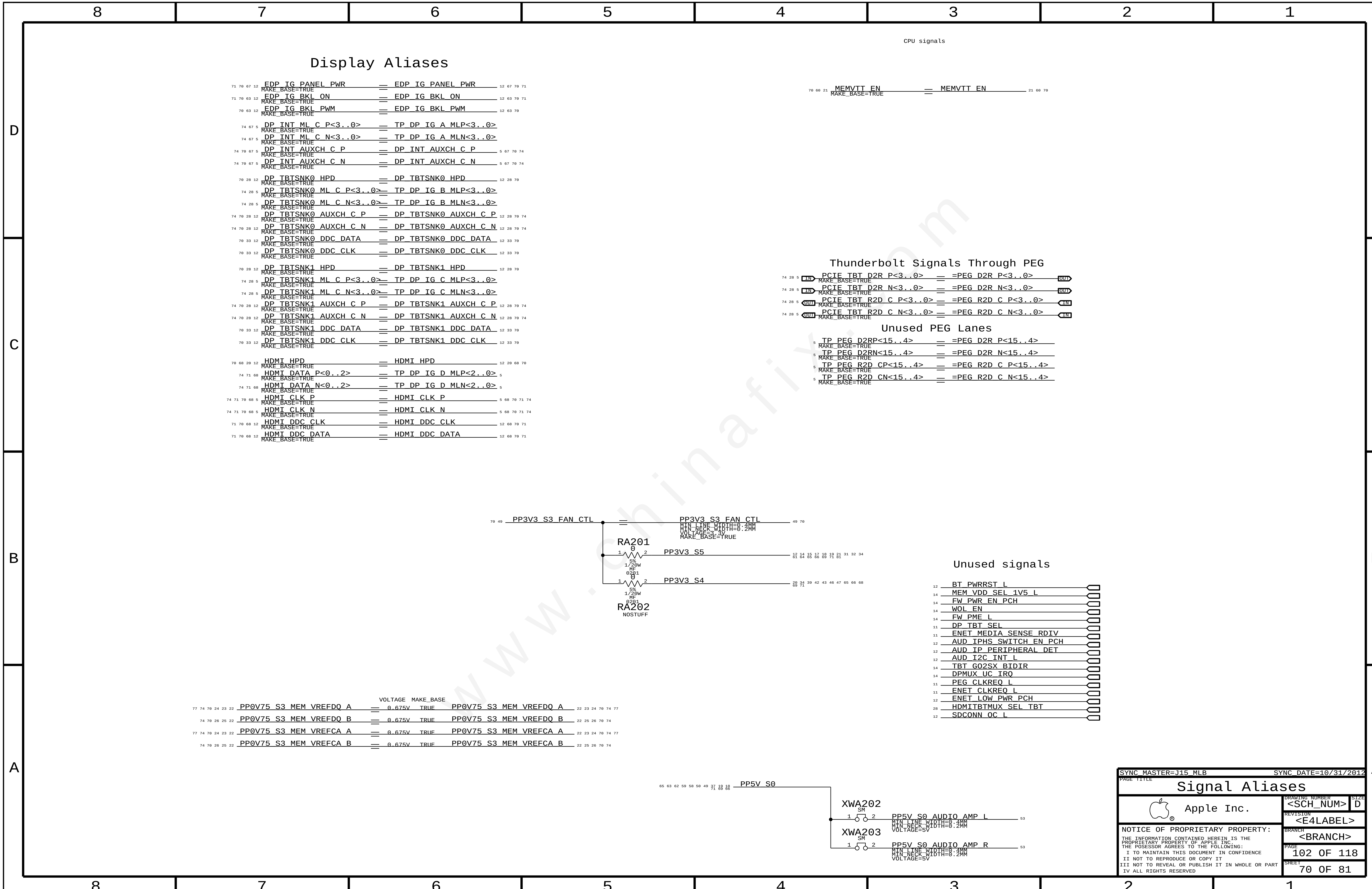
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G3H/5V Rails
3.3V Rails
1.5V/1.35V/1.05V/VCORE/BKLT Rails
TBT RAILS
PPBUS_G3H
PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_OTHER3V3_ISNS
PPVIN_S5_HS_OTHER5V_ISNS
PPVIN_S4_TPAD
PPDCIN_G3H
PPDCIN_G3H_ISOL
PP3V42_G3H
PPVRTC_G3H
PP5V_S5
PP5V_S4
PP5V_S3
PP5V_S0
PP3V3_S5
PP3V3_S4
PP3V3_SUS
PP3V3_S3
PP3V3_S0
PP3V3_S3RS0_CAMERA
PP1V35_S3
PP1V35_S3_MEM
PP1V35_S3RS0_CPUDDR
PP1V35_S3RS0_FET
PP1V5_S0
PPVTTDDR_S3
PPVTT_S0_DDR
PP1V05_SUS
PP1V05_S0
PPVCC_S0_CPU
PPBUS_SW_BKL
PP3V3_S4_TBT
PP3V3_S0SW_SSD_R
PP3V3_S0SW_SSD
PP3V3_TBTLC
PP15V_TBT
PPVIN_SW_TBTBST
VOLTAGE=12.8V
GND
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.085 MM
VOLTAGE=0V
MAKE_BASE=TRUE
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
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Power Aliases
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CPU signals
Display Aliases
EDP_IG_PANEL_PWR = EDP_IG_PANEL_PWR
EDP_IG_BKL_ON = EDP_IG_BKL_ON
EDP_IG_BKL_PWM = EDP_IG_BKL_PWM
DP_INT_ML_C_P<3..0> = TP_DP_IG_A_MLP<3..0>
DP_INT_ML_C_N<3..0> = TP_DP_IG_A_MLN<3..0>
DP_INT_AUXCH_C_P = DP_INT_AUXCH_C_P
DP_INT_AUXCH_C_N = DP_INT_AUXCH_C_N
DP_TBTSNK0_HPD = DP_TBTSNK0_HPD
DP_TBTSNK0_ML_C_P<3..0> = TP_DP_IG_B_MLP<3..0>
DP_TBTSNK0_ML_C_N<3..0> = TP_DP_IG_B_MLN<3..0>
DP_TBTSNK0_AUXCH_C_P = DP_TBTSNK0_AUXCH_C_P
DP_TBTSNK0_AUXCH_C_N = DP_TBTSNK0_AUXCH_C_N
DP_TBTSNK0_DDC_DATA = DP_TBTSNK0_DDC_DATA
DP_TBTSNK0_DDC_CLK = DP_TBTSNK0_DDC_CLK
DP_TBTSNK1_HPD = DP_TBTSNK1_HPD
DP_TBTSNK1_ML_C_P<3..0> = TP_DP_IG_C_MLP<3..0>
DP_TBTSNK1_ML_C_N<3..0> = TP_DP_IG_C_MLN<3..0>
DP_TBTSNK1_AUXCH_C_P = DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_N = DP_TBTSNK1_AUXCH_C_N
DP_TBTSNK1_DDC_DATA = DP_TBTSNK1_DDC_DATA
DP_TBTSNK1_DDC_CLK = DP_TBTSNK1_DDC_CLK
HDMI_HPD = HDMI_HPD
HDMI_DATA_P<0..2> = TP_DP_IG_D_MLP<2..0>
HDMI_DATA_N<0..2> = TP_DP_IG_D_MLN<2..0>
HDMI_CLK_P = HDMI_CLK_P
HDMI_CLK_N = HDMI_CLK_N
HDMI_DDC_CLK = HDMI_DDC_CLK
HDMI_DDC_DATA = HDMI_DDC_DATA
MAKE_BASE=TRUE
MEMVTT_EN = MEMVTT_EN
Thunderbolt Signals Through PEG
PCIE_TBT_D2R_P<3..0> = =PEG_D2R_P<3..0>
PCIE_TBT_D2R_N<3..0> = =PEG_D2R_N<3..0>
PCIE_TBT_R2D_C_P<3..0> = =PEG_R2D_C_P<3..0>
PCIE_TBT_R2D_C_N<3..0> = =PEG_R2D_C_N<3..0>
Unused PEG Lanes
TP_PEG_D2RP<15..4> = =PEG_D2R_P<15..4>
TP_PEG_D2RN<15..4> = =PEG_D2R_N<15..4>
TP_PEG_R2D_CP<15..4> = =PEG_R2D_C_P<15..4>
TP_PEG_R2D_CN<15..4> = =PEG_R2D_C_N<15..4>
PP3V3_S3_FAN_CTL = PP3V3_S3_FAN_CTL
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
RA201 0 5% 1/20W MF 0201
PP3V3_S5
RA202 0 5% 1/20W MF 0201 NOSTUFF
PP3V3_S4
Unused signals
BT_PWRRST_L
MEM_VDD_SEL_1V5_L
FW_PWR_EN_PCH
WOL_EN
FW_PME_L
DP_TBT_SEL
ENET_MEDIA_SENSE_RDIV
AUD_IPHS_SWITCH_EN_PCH
AUD_IP_PERIPHERAL_DET
AUD_I2C_INT_L
TBT_GO2SX_BIDIR
DPMUX_UC_IRQ
PEG_CLKREQ_L
ENET_CLKREQ_L
ENET_LOW_PWR_PCH
HDMITBTMUX_SEL_TBT
SDCONN_OC_L
VOLTAGE MAKE_BASE
PP0V75_S3_MEM_VREFDQ_A = 0.675V TRUE PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFDQ_B = 0.675V TRUE PP0V75_S3_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFCA_A = 0.675V TRUE PP0V75_S3_MEM_VREFCA_A
PP0V75_S3_MEM_VREFCA_B = 0.675V TRUE PP0V75_S3_MEM_VREFCA_B
PP5V_S0
XWA202 SM
PP5V_S0_AUDIO_AMP_L
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
XWA203 SM
PP5V_S0_AUDIO_AMP_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
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Signal Aliases
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Functional Test Points

FUNC_TEST J3501 - airport

- AP_CLKREQ_Q_L 34
- AP_RESET_CONN_L 34
- PCIE_AP_D2R_PI_N 34 76
- PCIE_AP_D2R_PI_P 34 76
- PCIE_AP_R2D_N 34 76
- PCIE_AP_R2D_P 34 76
- PCIE_CLK100M_AP_CONN_N 34 76
- PCIE_CLK100M_AP_CONN_P 34 76
- PCIE_WAKE_L 12 34 36 76
- PP3V3_S3RS4_BT_F 34
- PP3V3_WLAN 34 42
- USB_BT_CONN_N 34 75
- USB_BT_CONN_P 34 75
- WIFI_EVENT_L 34 41 42
- GND 4X

J4002 - Camera

- MIPI_CLK_CONN_N 37 79
- MIPI_CLK_CONN_P 37 79
- CAM_SENSOR_WAKE_L_CONN 37
- MIPI_DATA_CONN_N 37 79
- MIPI_DATA_CONN_P 37 79
- SMBUS_SMC_0_S0_SDA 37 41 44 48 80
- SMBUS_SMC_0_S0_SCL 37 41 44 48 80
- I2C_CAM_SCK 36 37
- I2C_CAM_SDA 36 37
- PP5V_S3RS0_ALSCAM_F 37
- GND

J9500 - rio coax

- HDMI_CLK_N 5 68 70 74
- HDMI_CLK_P 5 68 70 74
- HDMI_DATA_N<0> 68 70 74
- HDMI_DATA_N<1> 68 70 74
- HDMI_DATA_N<2> 68 70 74
- HDMI_DATA_P<0> 68 70 74
- HDMI_DATA_P<1> 68 70 74
- HDMI_DATA_P<2> 68 70 74
- USB3_SD_D2R_N 13 20 68 76
- USB3_SD_D2R_P 13 20 68 76
- USB3_SD_R2D_C_N 13 20 68 76
- USB3_SD_R2D_C_P 13 20 68 76
- USB3_EXTB_D2R_N 13 68 75
- USB3_EXTB_D2R_P 13 68 75
- USB3_EXTB_R2D_N 68 75
- USB3_EXTB_R2D_P 68 75
- USB_EXTB_N 13 68 75
- USB_EXTB_P 13 68 75
- GND 19X

J9510 - rio flex

- SD_PWR_EN 13 18 68
- PP1V5R1V35_S0_RIO 68
- HDMI_DDC_CLK 12 68 70
- HDMI_DDC_DATA 12 68 70
- HDMI_HPD_L
- SMBUS_PCH_CLK 13 18 22 44 63 68 76
- SMBUS_PCH_DATA 13 18 22 44 63 68 76
- PM_SLP_S3_BUF_L 51 65 66 68
- PM_SLP_S4_L 12 21 34 38 41 66 68
- PP3V3_S3 3X
- PP3V3_S4
- PP5V_S4 5X
- RIO_SDCONN_STATE_CHANGE_L 20 68
- USB_EXTB_OC_L 18 68
- GND 10X

J5150 - hall effect

- PP3V42_G3H
- SMC_LID_R 43
- GND

J6050 - left fan

- FAN_LT_PWM 49
- FAN_LT_TACH 49
- PP5V_S0 3X
- GND 5X

J6060 - right fan

- FAN_RT_PWM 49
- FAN_RT_TACH 49
- PP5V_S0 3X
- GND 5X

FUNC_TEST J6100 - lpc + spi

- LPCPLUS_GPIO 14 50
- LPCPLUS_RESET_L 20 50 76
- LPC_AD<0> 13 41 50 76
- LPC_AD<1> 13 41 50 76
- LPC_AD<2> 13 41 50 76
- LPC_AD<3> 13 41 50 76
- LPC_CLK33M_LPCPLUS 19 50 76
- LPC_FRAME_L 13 41 50 76
- LPC_PWRDWN_L 12 20 41 50
- LPC_SERIRQ 13 41 50
- PM_CLKRUN_L 12 41 50
- PP5V_S0
- SMC_RESET_L 41 42 50 57
- SMC_ROMBOOT 42 50
- SMC_RX_L 41 42 50
- SMC_TCK 41 42 50
- SMC_TDI 41 42 50
- SMC_TDO 41 42 50
- SMC_TMS 41 42 50
- SMC_TX_L 41 42 50
- SPIROM_USE_MLB 14 50
- SPI_ALT_CLK 50
- SPI_ALT_CS_L 50
- SPI_ALT_MISO 50
- SPI_ALT_MOSI 50
- TP_SMC_MD1 50
- TP_SMC_TRST_L 50
- GND 2X

J4800 - ipd flex

- Z2_CS_L 39
- Z2_MOSI 39
- Z2_MISO 39
- Z2_SCLK 39
- Z2_HOST_INTN 39
- Z2_CLKIN 39
- Z2_KEY_ACT_L 39
- PSOC_F_CS_L 39
- PICKB_L 39
- PSOC_MOSI 39
- PSOC_MISO 39
- PSOC_SCLK 39
- SMBUS_SMC_2_S3_SCL 39 41 44 80
- SMBUS_SMC_2_S3_SDA 39 41 44 80
- SMC_LID 39 41 42 43
- SMC_T101_COM_1
- PP3V3_S4
- PP5V_S5
- GND 2X

J4813 - keyboard

- PP3V3_S4
- PP3V42_G3H
- WS_CONTROL_KBD 39
- WS_KBD1 39
- WS_KBD10 39
- WS_KBD11 39
- WS_KBD12 39
- WS_KBD13 39
- WS_KBD14 39
- WS_KBD15_CAP 39
- WS_KBD16_NUM 39
- WS_KBD17 39
- WS_KBD18 39
- WS_KBD19 39
- WS_KBD2 39
- WS_KBD20 39
- WS_KBD21 39
- WS_KBD22 39
- WS_KBD23 39
- WS_KBD3 39
- WS_KBD4 39
- WS_KBD5 39
- WS_KBD6 39
- WS_KBD7 39
- WS_KBD8 39
- WS_KBD9 39
- WS_KBD_ONOFF_L 39
- WS_LEFT_OPTION_KBD 39
- WS_LEFT_SHIFT_KBD 39
- GND 2X

J4915 - kbd bklt

- KBDBKLT_RETURN1 2X 40 63
- KBDBKLT_RETURN2 2X 40 63
- PPVOUT_S0_KBDBKLT 40 63
- GND 4X

FUNC_TEST J6701 - audio flex

- AUD_HP_PORT_L 51 55
- AUD_HP_PORT_R 51 55
- AUD_SPDIF_OUT_JACK
- AUD_TIPDET_INV
- AUD_TYPEDET 51 55
- AUD_CONN_MIC_XW 4X
- CH_HS_MIC
- PP3V3_S0
- AUD_CONN_SLEEVE_XW 4X 54 55
- US_HS_MIC
- GND 2X GND

J6601 - mic

- DMIC_CLK3 52 55
- PP3V3_S0
- DMIC_SDA2 55
- DMIC_SDA3 52 55
- GND

J6602 - L speaker

- SPKRCONN_L_ID 52 55
- SPKRCONN_L_OUT_N 53 55 81
- SPKRCONN_L_OUT_P 53 55 81
- SPKRCONN_SL_OUT_N 53 55 81
- SPKRCONN_SL_OUT_P 53 55 81
- GND

J6603 - R speaker

- SPKRCONN_R_ID 52 55
- SPKRCONN_R_OUT_N 53 55 81
- SPKRCONN_R_OUT_P 53 55 81
- SPKRCONN_SR_OUT_N 53 55 81
- SPKRCONN_SR_OUT_P 53 55 81
- GND

J7000 - DC PWR

- ADAPTER_SENSE 56
- PP20V_DCIN_FUSE 2X 56
- GND 2X

J7050 - battery

- PPVBAT_G3H_CONN 8X 56 57
- SMBUS_SMC_5_G3_SCL 41 44 56 57 80
- SMBUS_SMC_5_G3_SDA 41 44 56 57 80
- SYS_DETECT_L 56
- GND 8X

J8300 - eDP

- DP_INT_AUX_N 67 74
- DP_INT_AUX_P 67 74
- DP_INT_ML_N<0> 67 74
- DP_INT_ML_N<1> 67 74
- DP_INT_ML_N<2> 67 74
- DP_INT_ML_N<3> 67 74
- DP_INT_ML_P<0> 67 74
- DP_INT_ML_P<1> 67 74
- DP_INT_ML_P<2> 67 74
- DP_INT_ML_P<3> 67 74
- LCD_FSS 63 67
- LCD_HPD_CONN 67
- LED_RETURN_1 63 67
- LED_RETURN_2 63 67
- LED_RETURN_3 63 67
- LED_RETURN_4 63 67
- LED_RETURN_5 63 67
- LED_RETURN_6 63 67
- PP5VR3V3_SW_LCD 3X 67
- PPVOUT_S0_LCDBKLT 63 67
- GND 16X

Power Rails

- PM_SLP_S3_L 12 21 41 66
- PPVTT_S0_DDR 21 27 60 69
- PP3V3_S0
- PP3V3_S3
- PP3V3_S5
- PP3V3_S5_AVREF_SMC 41 42
- PP3V42_G3H
- PP5V_S0
- PP5V_S3
- PP5V_S5 39 61 65 69 71
- PPBUS_G3H 30 45 56 57 63 69
- PPDCIN_G3H 56 57 69
- PPVCC_S0_CPU 6 8 10 46 59 69
- PPVTTDDR_S3 60 69
- PP3V3_S0SW_SSD 35 46 69
- PP1V5_S0
- PP1V35_S3 21 22 46 60 65 69

FUNC_TEST XDP

- XDP_CPU_TCK 6 18 74
- XDP_PCH_TCK 11 18
- XDP_CPU_TDI 6 18 74
- XDP_CPU_TDO 6 18 74
- XDP_CPUPCH_TRST_L 6 18 74
- XDP_CPU_TMS 6 18 74
- XDP_PCH_TMS 11 18
- XDP_PCH_TDI 11 18
- XDP_PCH_TDO 11 18
- XDP_CPU_PREQ_L 6 18 74
- XDP_CPU_PRDY_L 6 18 74
- PM_RSMRST_L 12 66 76
- PM_PCH_PWROK 12 19 76
- PM_SYSRST_L 12 19 41 76
- CPU_CFG<3> 6 18 74
- PP1V05_S0 14 15 17 18 42 62 66 69
- GND 2X GND

FUNC_TEST Power Sequence

- SMC_ONOFF_L 39 41 42
- PM_DSW_PWRGD 12 41 76
- ALL_SYS_PWRGD 18 19 41 58 66
- PM_PCH_SYS_PWROK 12 18 19 41 76
- PLT_RESET_L 12 18 20 21
- EDP_IG_PANEL_PWR 12 67 70
- EDP_IG_BKL_ON 12 63 70

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Functional Test Points

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

NC NO_TESTs

PCH

NO_TEST MAKE_BASE

Net	NO_TEST	MAKE_BASE	Net
NC_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
NC_USB3_EXTC_D2RN	TRUE	TRUE	NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP	TRUE	TRUE	NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN	TRUE	TRUE	NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP	TRUE	TRUE	NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP	TRUE	TRUE	NC_USB3_EXTD_R2D_CP
NC_PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN
NC_PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP
NC_PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
NC_PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP
NC_SATA_A_D2RN	TRUE	TRUE	NC_SATA_A_D2RN
NC_SATA_A_D2RP	TRUE	TRUE	NC_SATA_A_D2RP
NC_SATA_A_R2D_CN	TRUE	TRUE	NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP	TRUE	TRUE	NC_SATA_A_R2D_CP
NC_SATA_B_D2RN	TRUE	TRUE	NC_SATA_B_D2RN
NC_SATA_B_D2RP	TRUE	TRUE	NC_SATA_B_D2RP
NC_SATA_B_R2D_CN	TRUE	TRUE	NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP	TRUE	TRUE	NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN
NC_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP
NC_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP
NC_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN
NC_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP
NC_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP
NC_USB_EXTCN	TRUE	TRUE	NC_USB_EXTCN
NC_USB_EXTCP	TRUE	TRUE	NC_USB_EXTCP
NC_USB_SDN	TRUE	TRUE	NC_USB_SDN
NC_USB_SDP	TRUE	TRUE	NC_USB_SDP
NC_USB_WLANN	TRUE	TRUE	NC_USB_WLANN
NC_USB_WLANP	TRUE	TRUE	NC_USB_WLANP
NC_USB_6N	TRUE	TRUE	NC_USB_6N
NC_USB_6P	TRUE	TRUE	NC_USB_6P
NC_USB_7N	TRUE	TRUE	NC_USB_7N
NC_USB_7P	TRUE	TRUE	NC_USB_7P
NC_USB_EXTDN	TRUE	TRUE	NC_USB_EXTDN
NC_USB_EXTDP	TRUE	TRUE	NC_USB_EXTDP
NC_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN
NC_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP
NC_USB_IRN	TRUE	TRUE	NC_USB_IRN
NC_USB_IRP	TRUE	TRUE	NC_USB_IRP
NC_ITPXDP_CLK100MN	TRUE	TRUE	NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP	TRUE	TRUE	NC_ITPXDP_CLK100MP
NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L
NC_PCI_CLK33M_OUT2	TRUE	TRUE	NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3
NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1
NC_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2
NC_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3
NC_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L
NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK
NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA
NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L
NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP
NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN
NC_SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

NO_TEST MAKE_BASE

Net	NO_TEST	MAKE_BASE	Net
NC_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT
TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN
NC_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN
NC_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP
NC_PCIE_CLK100M_GPUN	TRUE	TRUE	NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP	TRUE	TRUE	NC_PCIE_CLK100M_GPUP
NC_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_ENETSDN	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
NC_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
NC_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
NC_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP
NC_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3
NC_USB_4N	TRUE	TRUE	NC_USB_4N
NC_USB_4P	TRUE	TRUE	NC_USB_4P

Flag	Net
TRUE	PCIE_TBT_R2D_P<3..0>
TRUE	PCIE_TBT_R2D_N<3..0>
TRUE	PCIE_TBT_D2R_C_P<3..0>
TRUE	PCIE_TBT_D2R_C_N<3..0>
TRUE	DMI_S2N_P<3..1>
TRUE	DMI_S2N_N<3..1>
TRUE	DMI_N2S_P<3..1>
TRUE	DMI_N2S_N<3..1>

PLACEABLE BEAD-PROBES FOR TBT

Net	Part	Ref	Property
TBT_A_R2D_C_P<1>	BEAD-PROBE	BPA535	NO_XNET_CONNECTION=TRUE
TBT_A_D2R_P<1>	BEAD-PROBE	BPA531	NO_XNET_CONNECTION=TRUE
TBT_A_D2R_N<1>	BEAD-PROBE	BPA532	NO_XNET_CONNECTION=TRUE

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: NC & No Test

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE
PCB Rule Definitions

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_P<3:0>	5 12 72
	DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_N<3:0>	5 12 72
	DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_P<3:0>	5 12 72
	DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_N<3:0>	5 12 72
	FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
	FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
I125	DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
I126	DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
	CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
	CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
I151	CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
	CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
I132	CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
I130	CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
I133	CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 71
	XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP	11 72
	XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN	11 72
	XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 71
	XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 71
	XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 71
	XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 71
	XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 18 71
	XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
	XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
I134	XDP_BDRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
I135	XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 71
I136	XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 71
	CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 41
	CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 42
	CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 41 42 58
I150	CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
	PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	6 14 42
	PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
	PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
	CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 58
	CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 58
	CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 58
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
I140	CPU_MEM_VREF		CPU_VREF	CPU_DIMMA_VREFDQ	7 22
I141	CPU_MEM_VREF		CPU_VREF	CPU_DIMMB_VREFDQ	7 22
I144	CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 77
I145	CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70
I146	CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 77
I147	CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	22 25 26 70
I153	PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	5 28 70
I152	PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	5 28 70
I154		CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 72
I155		CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 72
I156	PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 72
I158	PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 72
I157		CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	5 28 70
I159		CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	5 28 70

DP AUX NET PROPERTIES

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I243	DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	5 67 70
I244	DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	5 67 70
I166		DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
I167		DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
I231		DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	67
I232		DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	67
I234		DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
I233		DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
I246	DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	5 67 70
I245	DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	5 67 70
I171	DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	67 71
I170	DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	67 71

DP / HDMI NET PROPERTIES

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I211	HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>	68 70 71
I210	HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>	68 70 71
I213	HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P	5 68 70 71
I212	HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N	5 68 70 71
I235	DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 28 70
I236	DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 28 70
I237		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
I238		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
I239	DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	5 28 70
I240	DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	5 28 70
I241		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
I242		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
I223	TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28
I224	TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28
I228		DP_85D		DP_TBTSNK0_AUXCH_C_P	12 28 70
I229		DP_85D		DP_TBTSNK0_AUXCH_C_N	12 28 70
I227	TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28
I226	TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28
I225		DP_85D		DP_TBTSNK1_AUXCH_C_P	12 28 70
I230		DP_85D		DP_TBTSNK1_AUXCH_C_N	12 28 70

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: CPU Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
		SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 72
		SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 72
I272		SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 72
I271		SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 72
I299		SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 72
I298		SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 72
I300		SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 72
I301		SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 72
I213	PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_EXTA	USB_85D	USB	USB_EXTA_P	13 38
	USB_EXTA	USB_85D	USB	USB_EXTA_N	13 38
I245	USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	38
I244	USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N	38
I248	USB_EXTA	USB_85D	USB	USB_LT1_P	38
I249	USB_EXTA	USB_85D	USB	USB_LT1_N	38
	USB_NC	USB_85D	USB	NC_USB_EXTCP	13 72
	USB_NC	USB_85D	USB	NC_USB_EXTCN	13 72
I238	USB_NC	USB_85D	USB	NC_USB_SDP	13 72
I239	USB_NC	USB_85D	USB	NC_USB_SDN	13 72
I273		CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	38 41 42
I274		CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	38 41 42
	USB_SMC	USB_85D	USB	NC_USB_SMCP	72
	USB_SMC	USB_85D	USB	NC_USB_SMCN	72
I281	USB_NC	USB_85D	USB	NC_USB_6P	13 72
I282	USB_NC	USB_85D	USB	NC_USB_6N	13 72
I283	USB_NC	USB_85D	USB	NC_USB_7P	13 72
I284	USB_NC	USB_85D	USB	NC_USB_7N	13 72
	USB_EXTB	USB_85D	USB	USB_EXTB_P	13 68 71
	USB_EXTB	USB_85D	USB	USB_EXTB_N	13 68 71
I260	USB_NC	USB_85D	USB	NC_USB_EXTDP	13 72
I259	USB_NC	USB_85D	USB	NC_USB_EXTDN	13 72
	USB_BT	USB_85D	USB	USB_BT_P	13 34
	USB_BT	USB_85D	USB	USB_BT_N	13 34
		USB_85D	USB	USB_BT_CONN_P	34 71
		USB_85D	USB	USB_BT_CONN_N	34 71
I285	USB_NC	USB_85D	USB	NC_USB_IRP	13 72
I286	USB_NC	USB_85D	USB	NC_USB_IRN	13 72
I288	USB_TPAD	USB_85D	USB	USB_TPAD_P	13 39
I287	USB_TPAD	USB_85D	USB	USB_TPAD_N	13 39
I302		USB_85D	USB	USB_TPAD_R_P	39
I303		USB_85D	USB	USB_TPAD_R_N	39
	PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
I228	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 38
I231	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 38
I267		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
I265		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
I230	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	38
I229	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	38
I268		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 38
I266		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 38
I222	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 68 71
I223	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 68 71
I264		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
I262		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
I220	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	68 71
I221	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	68 71
I261		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 68
I263		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 68
I290	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 72
I291	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 72
I293		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 72
I292		USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 72
I295	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 72
I294	NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 72
I296		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 72
I297		USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 72

Clock Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I256	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
I255	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
I254		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
I253	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 37
I251	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
I250		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 41 50 71
	LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 41 50 71
	LPC_RESET_L	LPC_45S	LPC	LPCPLUS_RESET_L	20 50 71
	SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 18 22 44 63 68 71
	SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 18 22 44 63 68 71
	SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 44
	SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 44
	SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 44
	SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 44
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 52
		HDA_45S	HDA	HDA_BIT_CLK_R	11
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 52
		HDA_45S	HDA	HDA_SYNC_R	11
		HDA_45S	HDA	HDA_RST_R_L	11
	HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 52
	HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 52
	HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	52
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 52
		HDA_45S	HDA	HDA_SDOUT_R	11 19
		SPI_45S	SPI	SPI_CLK_R	13 50
	SPI_CLK	SPI_45S	SPI	SPI_CLK	50
		SPI_45S	SPI	SPI_MOSI_R	13 50
	SPI_MOSI	SPI_45S	SPI	SPI_MOSI	50
	SPI_MISO	SPI_45S	SPI	SPI_MISO	13 50
		SPI_45S	SPI	SPI_CS0_R_L	13 50
	SPI_CS0	SPI_45S	SPI	SPI_CS0_L	50
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	13 20 68 71
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	13 20 68 71
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	13 20 68 71
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	13 20 68 71
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	34 71
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	34 71
		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 34
I304		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 34
		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	34
I303		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	34
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 34
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 34
I275		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	34 71
I276		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	34 71
I325	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	36 37
I326	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	36 37
I327		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 37
I328		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 37
I329	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 37
I330	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 37
I331		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	36 37
I332		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	36 37
		CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 41
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 50 71
I293		CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
I298	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
I258	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
I260	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
I253	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
I254	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
I262	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
I261	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
I255	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
I257	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
I256	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
I259	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_P	
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_N	
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
I300		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	34 71
I299		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	34 71
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 37
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 37
I333		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	36 37
I334		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	36 37
I281	PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
I282		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I313	PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
I314	PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
I315	PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
I316	PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
I308	PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 66 71
I307	PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 41 71
I318	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
I317	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
I320	PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 41 71
I319	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 41 71
I321	PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 41
I322	PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 42
I323	PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 34 36 71
I324	PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
I335	PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_P<3..0>	13 35
I336	PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_N<3..0>	13 35
I338	PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_P<3..0>	13 35
I337	PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_N<3..0>	13 35
I339		PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_P<3..0>	35
I340		PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_N<3..0>	35

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: PCH Constraints 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

		NET_TYPE			
	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET	PAGES
	MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	7 23 27
	MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	7 23 27
I130	MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1>	7 24 27
I129	MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1>	7 24 27
	MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0>	7 23 27
I124	MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1>	7 24 27
I125	MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0>	7 23 27
I101	MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1>	7 24 27
I126	MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 23 27
I103	MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1>	7 24 27
	MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	7 23 24 27
	MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	7 23 24 27
	MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	7 23 24 27
	MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	7 23 24 27
	MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	7 23 24 27
	MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 23 24
	MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 23 24
	MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 23 24
	MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 23 24
	MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 23 24
	MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 23 24
	MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 23 24
I105	MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 23 24
I106	MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 23 24
	MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 23 24
	MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 23 24
	MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 23 24
	MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 23 24
	MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 23 24
	MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 23 24
	MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 23 24
	MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 23 24
	MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 23 24
	MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 23 24
	MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 23 24
I117	MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 23 24
I118	MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 23 24
I116	MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 23 24
I119	MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 23 24
	MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	7 25 27
	MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	7 25 27
I127	MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1>	7 26 27
I128	MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1>	7 26 27
	MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0>	7 25 27
I120	MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1>	7 26 27
I121	MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0>	7 25 27
I122	MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1>	7 26 27
I123	MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 25 27
	MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1>	7 26 27
I108	MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	7 25 26 27
	MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	7 25 26 27
	MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	7 25 26 27
	MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	7 25 26 27
	MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	7 25 26 27
	MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 25 26
	MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 25 26
	MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 25 26
	MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 25 26
	MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 25 26
	MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 25 26
	MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 25 26
	MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 25 26
	MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 25 26
	MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 25 26
	MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 25 26
	MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 25 26
	MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 25 26
	MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 25 26
	MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 25 26
	MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 25 26
	MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 25 26
	MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 25 26
	MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 25 26
	MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 25 26
I113	MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 25 26
I112	MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 25 26
I115	MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 25 26
I114	MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 25 26
I110			MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 74
I109			MEM_PWR	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 74
I111			MEM_PWR	PP1V35_S3_MEM	23 24 25 26 46 69

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0>	28 31 72
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0>	28 31
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0>	31
	TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0>	31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	28 31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	28 31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	31
	DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	31
I308	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	28 31
I310	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	28 31
I311	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	31
I309	DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0>	31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0>	31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0>	28 31
	TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0>	28 31
I312	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1>	31
I313	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1>	31
I314	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1>	28 31 72
I315	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1>	28 31 72
	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P	31
	TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N	31
	TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P	28 31
	TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N	28 31
	TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P	31
	TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N	31

Only used on dual-port hosts.

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I316	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0>	28 32
I317	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0>	28 32
I318	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0>	32
I319	TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0>	32
I321	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	28 32
I322	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	28 32
I320	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	32
I324	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	32
I325	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	32
I323	DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	32
I327	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	28 32
I326	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	28 32
I328	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	32
I329	DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	32
I331	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0>	32
I332	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0>	32
I330	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0>	28 32
I334	TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0>	28 32
I333	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1>	32
I336	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1>	32
I337	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1>	28 32
I335	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1>	28 32
I339	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P	32
I338	TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N	32
I341	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P	28 32
I340	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N	28 32
I342	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P	32
I343	TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N	32

Thunderbolt IC Net Properties

Only used on hosts supporting Thunderbolt video-in

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	28

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	36 37
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	36 37
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	36 37
I101	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	36 37
I102		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	37
I103	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	36 37
I104	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	36 37
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	36 37
I106	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	36 37
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	36 37
I108	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	36 37
I107	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	36 37
I109	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	36 37
I110	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	36 37
I147	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	36 37
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	36 37
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	36 37
I127	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	36 37
I128	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	36 37
I129		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	37 71
I130		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	37 71
I134	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	36 37
I133	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	36 37
I132		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	37 71
I131		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	37 71
I145			S2_MEM_PWR	PP1V35_CAM	36 37
I146			S2_MEM_PWR	PP0V675_CAM_VREF	36 37
I148			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	37
I149			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	37

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	Pages
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	39 41 44 71
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	39 41 44 71
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	41 44 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	41 44 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	37 41 44 48 71
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	37 41 44 48 71
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	41 44 56 57 71
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	41 44 56 57 71
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	41 43
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	Pages
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
I426	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P	47
I425	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N	47
I421		THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P	47
I423		THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N	47
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P	48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N	48
I422	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_P	47
I424	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_N	47
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P	48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N	48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P	48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N	48
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P	46
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N	46
I419		SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P	46
I420		SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N	46
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	
		SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P	47
		SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N	47
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	47 63
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	47 63
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P	45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N	45
I514	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P	45
I515	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N	45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	45
		SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P	46
		SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N	46
I510	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	
I511	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	
I429	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P	46 59
I430	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N	46 59
I433	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P	46 59
I434	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N	46 59
I435	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P	46 59
I431	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N	46 59
I432	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P	46
I436	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N	46
I498	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	81
I499	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	81
I502	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	81
I503	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	81
I405	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	46
I406	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P	46
I407		AUDIODIFF	AUDIO	ISNS_TBT_R_N	46
I408		AUDIODIFF	AUDIO	ISNS_TBT_R_P	46
I446	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P	46
I445		THERM_1TO1_45S	THERM	ISNS_SSD_N	46
I447	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P	46
I448		THERM_1TO1_45S	THERM	ISNS_SSD_R_N	46
I449	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P	62
I450		THERM_1TO1_45S	THERM	P1V05S0_CS_N	62
I451	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE_P	62
I452		THERM_1TO1_45S	THERM	P1V05S0_SENSE_N	62
I453	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P	28 48
I454		THERM_1TO1_45S	THERM	TBT_THERMD_N	48
I455	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P	57
I456		AUDIODIFF	AUDIO	CHGR_CSI_R_N	57
I457	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P	57
I458		AUDIODIFF	AUDIO	CHGR_CSO_R_N	57
I517	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P	
I516	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N	
I519	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P	47
I518	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N	47

J15 Specific Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
I361		AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
I362		AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
I459		AUDIODIFF	AUDIO	RSUBIN_P	53
I440		AUDIODIFF	AUDIO	RSUBIN_N	53
I441		AUDIODIFF	AUDIO	LSUBIN_P	53
I442		AUDIODIFF	AUDIO	LSUBIN_N	53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
		AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
I461		AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
I462		AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
I460		AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
I463		AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
I358	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	53 55 71
I357	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	53 55 71
I360	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	53 55 71
I359	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	53 55 71
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	53 55 71
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	53 55 71
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	53 55 71
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	53 55 71
I480	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P	
I481	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N	
I482	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P	51
I483	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N	51
I484	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P	
I485		DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N	
I486		DIFFPAIR	AUDIO	AUD_HS_MIC_P	54 55
I487		DIFFPAIR	AUDIO	AUD_HS_MIC_N	54 55
I489		DIFFPAIR	AUDIO	HS_MIC_P	51 54
I488		DIFFPAIR	AUDIO	HS_MIC_N	51 54
I490		DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P	
I491		DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N	
I494	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	51 53
I495	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N	51 53
I493	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	51 53
I492	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N	51 53
			SB_POWER	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 61 64 65 66 69 70 71
			SB_POWER	PP3V3_S0	65 66 67 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55 69 71
			SB_POWER	PP1V35_S3RS0_CPUDDR	6 8 10 21 65 66 69
			GND	GND	

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